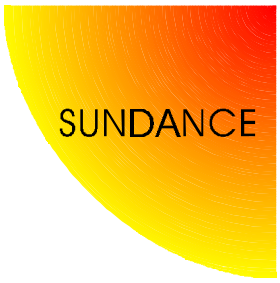
SMT103



User Manual
Version 2.0

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Sundance now operate a World Wide Web page, and information is posted on a regular basis to provide our customers with the most up to date information concerning our products.

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Chapter 1 General Introduction

The INMOS pioneered, Parallel Processing standard is built around that of the TRAM (**TRA**nsputer **M**odule) concept, which consists of a variety of module sizes. These vary from the smallest size 1 (3.66"x1.05"') to the largest size 8 (3.66" x 8.40"). TRAMs may contain a transputer, some memory and other various I/O functions. These may include Analog to Digital converters; IEEE interfaces; SCSI controllers, and high resolution graphics devices.

The TRAM format has also been used by many manufacturers to integrate sequential processors like Intel's i860 Vector processor, Motorola's 56000/96000 DSP, Zoran's Vector DSPs and AT&T's DSPs into transputer networks. The only other truly parallel processing processor, Texas Instruments TMS32C40 pDSP, has also been incorporated into a TRAM format using a size 4 board.

The recently launched INMOS T9000 transputer will also be supported by the current TRAM specification, although INMOS have upgraded the standard to the HTRAM, using a hard metric format. Despite this newly adopted standard, INMOS have said that they will launch a few products using the T9000 in the original TRAM format. A resemblance to the PC industry, where the PC/ATs are the more widely used and therefore cheapest, but the MCA/EISA standard is the newer, faster and more expensive product. Sundance will support both, although our first product, SMT209, will be a size 4 TRAM.

The front-end computer host system for transputers and TRAMs span from minimum PC/XTs to high-end SUN and VAX workstations. They all have a basic common interface protocol, the INMOS AFServer, with different hardware implementations. This protocol was introduced by INMOS with their first product for the PC, the INMOS B004 PC plug-in board. The INMOS B004 standard was extended with the arrival of the TRAM concept and the INMOS B008 10-slot TRAM motherboard for the PC.

The SMT103 is an entry level, cost-effective TRAM motherboard, and integrated transputer system. It can take up to four size 1 TRAMs, in addition to the onboard transputer and memory system. This onboard system can support up to 16 MBytes of dynamic memory with a 20, 25 or 30 MHz transputer. The TRAM slots allow the user to experiment with parallel processing. Any combination of sizes, up to and including size 4 can be used. Compatibility with the INMOS B004 industry standard, support of both the SubSystem, Up and Down Reset, Analyse and Error protocols, provide the user with maximum flexibility and value for money.

Highly integrated component usage on the PC interface, and extensive use of surface mount technology has enabled the SMT103 to be condensed onto a board no bigger than a standard 8-bit interface card. This form factor will allow the SMT103 to be used in most old PC/XTs desktop computers and current generation laptop and notebook computers. This feature enables even the oldest IBM PCs and all ISA Bus based PC users to either experiment with parallel processing or take advantages of applications written for small scale parallel processing using transputers and TRAMs. It is also possible to use other processor types from other manufactures if their interface matches that of TRAMs.

At the other end of the application scene, the SMT103 can be utilised in a large scale parallel processing environment, as all the unique INMOS transputer Link connections are brought to the back panel of the PC for easy access. In the extreme, a network of

hundreds of SMT103s, each with more than 50Mflops of performance, could be constructed in this way.

To maximise the configurations that the board can be used in there are sets of jumpers on the board. These links set various options, ranging from the speed of the link interfaces to the address of the board in the host's memory map. These functions will be described in detail in a later section. The board has been designed to meet the requirements of B004 compatibility. This allows existing software to run on the board without any modification.

The SMT103 is manufactured by Sundance Multiprocessor Technology Limited, a high quality manufacturer of parallel processing products. It is covered by a one Year, return to factory, warranty from the date of purchase.

Box Contents

When the SMT103 is shipped, the box contains other parts that are useful in configuring the system. There is this manual. All the sections in this manual should be read before any attempt is made to install the board. There will also be a bag of pipe jumpers and pinstrips. These can then be used as spacers for any TRAMs that require some clearance from the motherboard.

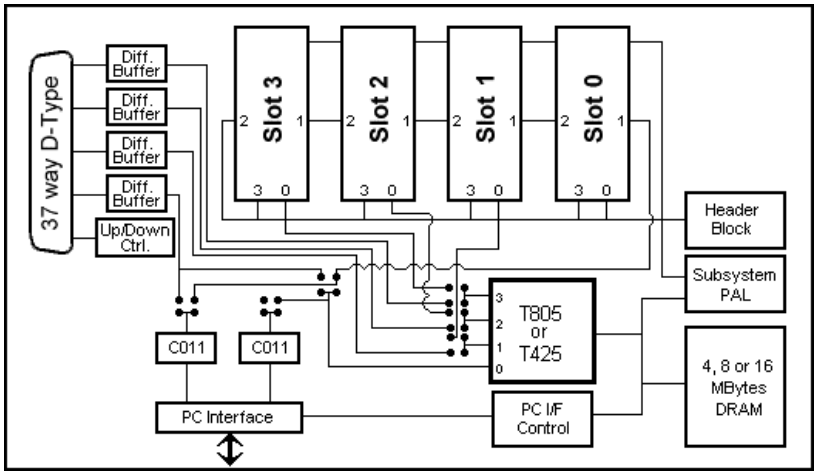


Figure 1: Functional block diagram

Chapter 2 Installation

Unpack the SMT103 from its container and inspect it visually. If there is any sign of damage to the board or components then go no further, but inform the carrier and your dealer. When delivered, the SMT103 is configured to use the speed and type of transputer, also the amount and speed of memory that was ordered; So no jumper adjustment should be needed at this point.

Turn off and disconnect the power from your IBM PC-XT, AT, or clone. Consult the manual supplied with your PC for instructions on how to insert add-in circuit boards. Insert the SMT103 into any convenient 8-bit card slot. Replace the PC cover or casing and reconnect the power and turn on.

Observe normal anti-static handling precautions when working with all electronic circuits. If one is available, use a wrist-strap grounding system. If not, then always touch a properly grounded bare metal surface BEFORE handling any circuit. Also avoid all contact with connector pins on plug in cards and components. TRAMs can easily sustain mechanical damage, the connector pins are easily bent by misalignment with their sockets on insertion, or by dropping them. The pins are expensive to replace, and on some boards they are impossible to remove. Many TRAMs that can be purchased use surface mount technology. These types of components are fragile. They can easily be ripped off the surface of the PCB by very rough handling.

Prepare the board by inserting your choice of transputer modules, connecting the links and checking the jumper settings.

Prepare the Host PC and insert the board

1. Turn off the power to your PC and remove the system unit cover following the instructions supplied with your system. If in doubt, consult your dealer.
2. Select a slot in your PC. Remember that you only need to use an 8-bit slot. When you are deciding which slot to use please note that some TRAMs have a very high profile. You may not be able to place your board in a slot next to another slot that already has a board in it. Take care to ensure that the TRAMs do not foul on the underside of any existing boards.
3. Remove the metal blanking plate from the aperture in the system box that will hold the SMT103 connector.
4. Insert the SMT103 into the PC, holding it true both vertically and horizontally to avoid catching any adjacent cards.
5. Push the SMT103 firmly into the PC connector. Apply careful but firm pressure to the top centre of the card. **Do not press on the modules or components**.
6. Replace the PC cover and reconnect the system to the power.

Chapter 3. Fitting the TRAMs

Handling Precautions

Observe normal anti-static handling precautions when working with all electronic circuits. If one is available, use a wrist-strap grounding system. If not, then always touch a properly grounded bare metal surface BEFORE handling any circuit. Also avoid all contact with connector pins on plug in cards and components.

TRAMs can easily sustain mechanical damage, The gold connector pins are easily bent by misalignment with their sockets on insertion, or by dropping them. The pins are expensive to replace, and on some boards they are impossible to remove. Many TRAMs that can be purchased use surface mount technology. These types of components are fragile. They can easily be ripped off the surface of the PCB by very rough handling.

Which slot(s) to use

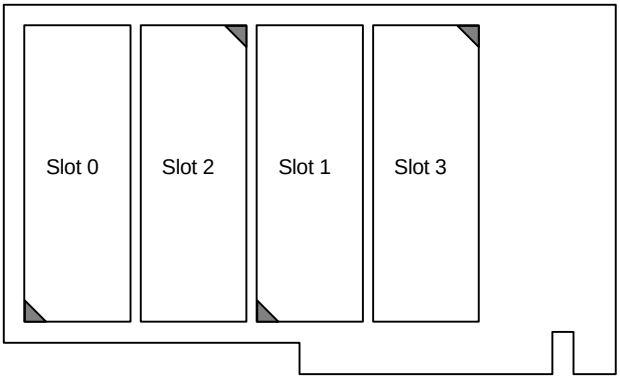


Figure 2. TRAM slot positions

Please refer to figure 2 for a map of the positions, orientation and numbering of the TRAM slots. Usually the first TRAM fitted to the board will go into slot 0.

If all of the TRAM slots are not filled then small link jumpers will have to be fitted to the TRAM slots. This is so the link pipe remains continuous. If however, you are not worried about information coming into the board at the other end of the pipe network then this can be ignored.

How to fit a TRAM

1. Decide which slot to use. Conventionally, slots are filled in order. This may not be possible with different size TRAMs. You may have to experiment.
2. Remove any pipe jumpers that are fitted in the slot you wish to use.
3. TRAMs should have a white or yellow triangle marked on the printed circuit board in the corner by pin 1. Match this up with the pin 1 triangle on the SMT103. If there is no triangle marked on the TRAM then please consult the manufacturer's manual or the board supplier. The effort may well save you damaging the TRAM.
4. Most TRAMs are supplied with extension pins fitted to the strip sockets to protect them in transit. Remove them with a small pair of pliers or tweezers and store them safely. You will need to use them if the TRAM ever has to be returned for repair. Take great

care not to bend the pins soldered to the TRAM. If you are stacking one TRAM on top of another then keep the extenders in place.

5. Line up all the TRAM pins visually before inserting them in the motherboard sockets. When you are quite sure that the pins are aligned and partially inserted, the TRAM will push home with gentle but firm pressure.

Removal is the reverse of fitting. The TRAMs will have to be gently levered out using a small screwdriver. Be careful not to bend the TRAM pins.

Chapter 4 Using the SMT103

The SMT103 can be used in several ways and the rear DB37 socket and jumper blocks have to be arranged to suit each task. Three of the possibilities are described in the following sections.

On board transputer controlled by the host PC.

This is when the SMT103 is used in a machine in a stand alone configuration. In this mode all of the signals required to control the transputer are provided by the bus interface. This is referred to as the **B004 compatible interface**. The first ever transputer board to be used in a PC machine had the part number **B004,** and was produced by INMOS [2]. Since then all the other board manufacturers have produced compatible interfaces so that the software interface to the transputer remains compatible.

This configuration is the one required for the board to be able to be used with any of the stand alone software packages, such as the Inmos TDS and the 3L compilers. In this configuration the SMT103 can control external networks via either the *SubSys*- port or the *DownNot*- port. For a fuller description of these two interfaces see chapter 5.

In this mode no external connections have to be made to the DB37 socket on the back edge of the board. When the board is shipped to the customer all of the jumpers will be set to the positions required for this operation. (See appendix A)

Controlled by an external system

To control the onboard transputer from an external source then the jumper settings will have to be changed from those given in the first example. If you switch over the positions of JD1, JD2 and JD3 then the *Reset*, *Analyse* and *Error* lines on the transputer are connected to the *UpNot*- lines on the DB37 socket. The transputer can then be controlled from an external host. The Link connections have not been changed in any way.

If you wish to actually boot the transputer as part of an external network then one of the link lines on the DB37 will have to be connected to the external host. Link 0 remains connected to the host machine. This allows the transputer to access data on the host and then transmit it to some external source. This can only be done if you have the right software running on the host machine and transputer.

Use of the PClink and the PCNot- port alone.

The PCNot lines are connected directly to the DB37 connector. This allows the board to directly control an external transputer network. For a Link connection from the bus interface to be connected to the differential drivers the second C011 has to be fitted to the board and the links have to be set as shown in the second example in Appendix A.

Chapter 5 Switches

The SMT103 has a formidable number of links and jumpers. This chapter explains all of these links and their functions. Some examples of system configuration are given, however not all eventualities are explained. If you are having problems trying to get the system to operate in the way you think it should then please contact your supplier. Please read this chapter through several times before you try to make any changes to the board, and make a note of how the links are set now. The board will have been shipped set up for the configuration you ordered.

To help the user with jumper identification the following colour scheme has been adopted :-

Links	Colour
JD1, JD2, JD3, JRF, J4, J5, J6, J7, J8, J9, J16 and J17	Red
JF1, JF2, JF3, JF4, JF5, JF6, JF7, JF8, J10, J11, J12, J13, J14 and J15	White
JLS1, JLS2, JS1 and JS2	Black
TJ1, TJ2, TJ3, JMS and JCS	Blue

Table 1. Jumper colour allocation.

Transputer and TRAM Link Speed Selection

The transputer fitted on the SMT103 has four links that may be connected to other Inmos Link interfaces, either from other transputers or link adapters. The transmission speed of these links are set by jumper links JLS1 and JLS2. These link speed jumpers also set the link communication speed for the TRAM slots. To avoid invalid communication settings, both of the links should be placed the same way round. See figure 3 for details. Both of these links have to be set in the same direction otherwise the Links will fail to operate.

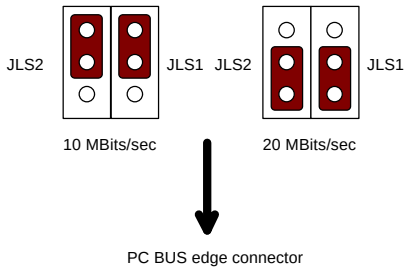


Figure 3. Transputer link speed

C011 Link Speed Selection

As well as being able to select the communications speed of the transputer and the TRAM slots it is also possible to select the speed of the C011's. There are optionally two of these devices fitted on the board. You will nearly always need the first device as it provides the main communication with the PC. The second device is the optional one. It allows a second set of ports to be decoded on the PC bus, and then used to communicate directly with the TRAM slots. You will need specialist software to be able to make use of this feature as standard servers do not expect to have two communicating systems in the

same machine. The link speed for these two devices are selected together and is selected via jumper JCS. See figure 4 for details.

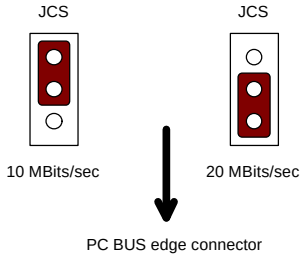


Figure 4. C011 Link speed selection

Transputer Clock Speed Selection

For completeness of information jumpers JS1 and JS2 set the clock speed of the transputer. The processor is soldered onto the board so cannot be changed. Leave these jumpers in the factory default settings.

Transputer Memory Speed Selection

Jumper JM5 is used to set the memory access speed of the processor. As neither the transputer or the DRAMs are user replaceable parts do not change this setting from the factory default.

The Internal Reset, Analyse and Error lines

The internal Reset, Analyse and Error lines on the board can be controlled by several sources. Also the lines going to the TRAM slots can be controlled from a different source to the main transputer.

Transputer lines Reset, Analyse and Error

The following paragraphs explain how the Reset, Analyse and Error lines for the onboard transputer are controlled. Please note that all of the signals should be set to the same source, or the board will fail to function as you expect it to.

The Reset line for the transputer can be directly controlled by one of two sources, and is selected by using jumper link JD1. It can be controlled by either the PCNot- control lines or the UpNot- control lines from the DB37 edge connector. The PCNot lines are controlled by the bus interface registers and these are described later.

Like the Reset line, the Analyse line can be controlled by either the UpNot- control lines or the PCNot- control lines. The selection is controlled by jumper link JD2.

Unlike the Reset and Analyse lines, the Error line is an output rather than an input. Jumper link JD3 is used to select the destination of the error line from the transputer.

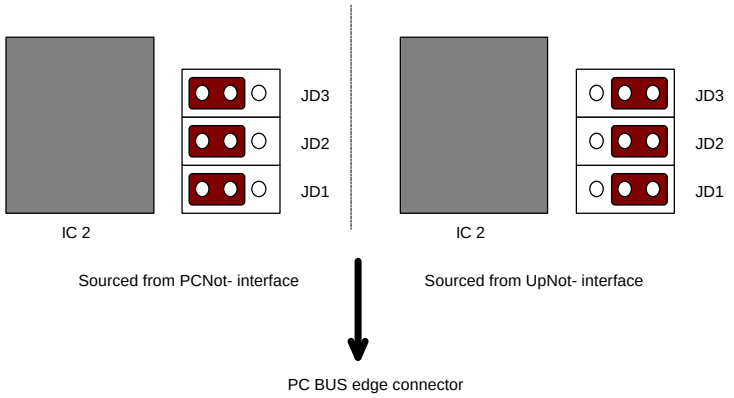


Figure 5. Reset, Analyse and Error Selection

Reset Propagation

On the B004 standard interface, when the on board transputer is reset then this is propagated through to the *SubSystemReset* line. This ensures that any network of transputers that is being controlled by the transputer are reset when it is reset. There are some instances when this feature is not desirable. To get around this, we have incorporated another link on the SMT103. JRF is used to either enable this compatibility or allow the board to prevent the RESET and ANALYSE signals being passed on to the SubSystem port

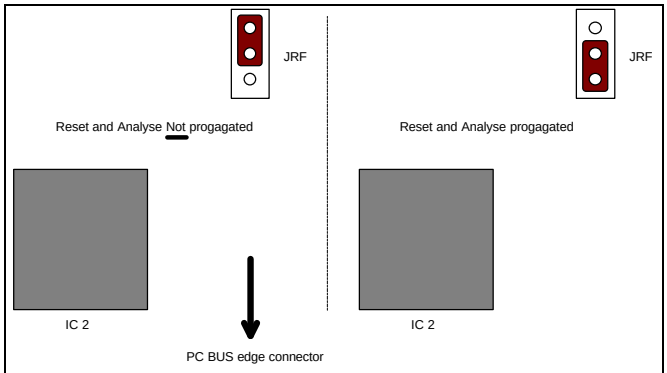


Figure 6. Reset and Analyse propagation

TRAM slots

The SMT103 has 4 size 1 TRAM slots as well as the on-board transputer. This allows the board to be used to develop a true parallel processing environment for use within a PC. The Reset, Analyse and Error lines for these slots can be controlled from one of two sources. They can either be connected to the lines that control the onboard transputer, whatever they are selected to be, or they can be connected to the SubSystem lines from the onboard transputer. The two options are shown in figure 7. Reset is controlled by TJ1, Analyse by TJ2 and Error by TJ3.

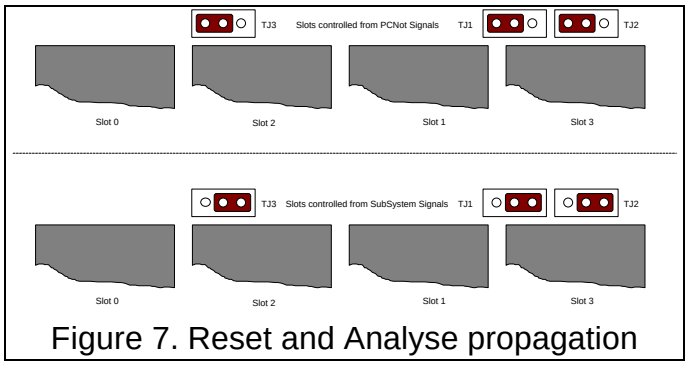


Figure 7. Reset and Analyse propagation

Chapter 6. Programmable Registers

On the SMT103 there are two sets of software registers. Some of these registers are only accessible from the PC host and the others are only accessible to the transputer.[1]

PC Registers

These are the registers that are only accessible from the PC host and are mapped as IO ports. Those on the PC host perform various control functions required for link communication, as well as allowing the user to control the status of external transputer networks.[2]

Input data registers, Output data registers

Address	Register
#150 & #200	Input Data Register (ro)
#151 & #201	Output Data Register (wo)
#152 & #202	Input Status Register (rw)
#153 & #203	Output Status Register (rw)
#160 & #210	Error Register (ro)
#160 & #210	Reset Register (wo)
#161 & #211	Analyse Register(wo)

Table 2. PC Port IO Map

These two registers are located inside the C011 chips, one set per device. The functions of the input data register and output data register are fairly obvious. When the status registers indicate that they are either ready to receive valid data, or they contain valid data then the data is written to or read from these registers.

Input Status registers, Output Status registers

These registers are contained in the C011 chips, one set per device and indicate the status of the input and output data registers. See table 3 for further information.

rd	Bit 0	"0" no input data [output not ready]
		"1" valid input data [output ready]
wr	Bit 1	"0" disable input [output] interrupt
		"1" enable input [output] interrupt

Table 3. Input [output] Status Register

Error Register

This is a software readable port that indicates the Error status of the transputer network connected to the *PCNotError* line. JD3 determines what error source is connected to this

[1] Throughout this document, any numbers prefixed with a # indicate that the number is hexadecimal.

[2] It is possible to provide boards with custom decoding in the ranges #150, #200 and #300 providing only one C011 is fitted, and it is requested when ordering.

line. It can either be the error line from the onboard transputer, or the *UpNotError* line from an external network of transputers. If the TRAMS are controlled by the PCNot-interface, then the TRAM error line is "ored" into this signal to provide the result given in the register. See page 13 for further details.

rd	Bit 0	"0" Error false
		"1" Error true

Table 4. Error Register

Reset Register

This register can be written to control the state of the *PCNotReset* line on the DB37 socket. This can then be used to control an external transputer network, as well as the onboard transputer. See table 5 for further information. JD1 is used to set the source of the *Reset* line used by the transputer. See page 13 for details as to where this signal will be routed.

wr	Bit 0	"0" Reset [Analyse] false
		"1" Reset [Analyse] true

Table 5. Reset Register

Analyse Register

This register can be written to control the state of the *Analyse* line of the onboard transputer, or the *PCNotAnalyse* line on the DB37 socket. Jumper JD2 is used to set the destination of this signal. See table 5 for more information on the programmable values for this register. See page 13 for details as to where this signal will be routed.

Transputer Accessible Registers

In the transputer section of the board there are three software addressable registers for controlling the *SubSystem* control lines that appear on the DB37 socket. These signals can then be used by the transputer on the SMT103 to control an external network of transputers, as well as the TRAM slots if so selected. Table 6 gives the addresses of these ports. They are BYTE registers placed on WORD boundaries.

Physical Address	Occam Address	Register
#00000000	#80000000	Error Register(ro)
#00000000	#80000000	Reset Register (wo)
#00000004	#80000004	Analyse Register (wo)

Table 6. SubSystem Address Map

SubSystem Error Register

This register can be used to monitor the status of any transputers that are connected to the *SubSysNotError* line on the DB37 socket. For information on the bit assignment in this register see table 7. If TJ3 is selected for this option then the register will also monitor the state of the TRAM error line. See page 14 for further information.

rd	Bit 0	"0" Error false
		"1" Error true

Table 7. SubSystem Error Register

SubSystem Reset Register

This register can be used to control the status of the *SubSysNotReset* line on the DB37 socket. This then gives the onboard transputer the ability to reset an external network of transputers, without affecting the state of any transputers that are connected to its *DownNot*-control pipeline. For information on the bit assignment in this register see table 8. If TJ1 is set to select this option then this register will also control the state of the TRAM reset line. For more information see page 14.

rd	Bit 0	"0" Reset [Analyse] false
		"1" Reset [Analyse] true

Table 8. SubSystem Reset [Analyse] Register

SubSystem Analyse Register

This register behaves in the same way as the Reset register except it effects the state of the *SubSysNotAnalyse* Line. For information on the bit assignment in this register see table 8. If TJ1 is set to select this option then this register will also control the state of the TRAM analyse line. For more information see page 14.

Example Code

This is a small piece of pseudo-code to demonstrate how to access the data registers on the PC Bus.

```
read_byte()
  do
    nothing
  while((read_status_port AND 1) equals 0)
  read in the input_data_port
  return the data read in

write_byte()
  do
    nothing
  while((write_status_port AND 1) equals 0)
  output data to output_data_port
 return
```

Chapter 7. What are Reset, Analyse and Error?

These three signals are used to control the operation of the transputer. Their names pretty well describe their functions in the system. The Reset line does exactly what it suggests. It is used to Reset transputers. When the signal is true, whatever transputers are connected to the signal are put into the reset state. They immediately stop processing and go into an idle state. When this signal is taken not true, how the transputer behaves will depend on the state of the Analyse line. If this line is also Not True then the transputer will initiate the boot process and then go into either the idle state and wait for a message on one of its links, or boot code from EPROM space. If the Analyse signal is true when the Reset line is taken Not True then the transputer will not perform any of the memory configuration read cycles, or any initial DRAM refresh cycles, but will enter a halted state. It will then remain in the halted state until it is told to do otherwise. For more detailed information read the Inmos T425/T805 etc. technical data sheets.

The Analyse line can be used to debug transputers whilst they are operating. If the Analyse line is taken True without the Reset line being taken True as well then the transputer will try to enter a halt state. It will enter the halt state at the next descheduling point. From Analyse being taken True the transputer will halt within 3 time slice periods plus the time taken for any high priority process to complete. As much of the transputer state is saved to allow remote transputers to debug the internal state of the transputer when it was halted. After Analysing a transputer it must be Reset otherwise its state is undefined. For more detailed information read the Inmos T425/T805 etc. technical data sheets.

The Error line indicates the error status of any transputer. This output from the transputer can be set either directly from software control, or as a result from performing instructions that generate error conditions. For a complete list of instructions, and how they may cause error conditions refer to the Inmos T425/T805 etc. technical data sheets.

Up and Down signals

The UpNot- and DownNot- control lines allow transputer boards to be configured into a pipeline. The Up signals from one board are connected to the Down signals coming from the previous board in the pipe. This then allows a pipe controller to issue Reset and Analyse signals to other transputers. It will send the valid signals out through its Down connector. These are then fed into the Up inputs in the next transputer in the pipe. This is then repeated for the entire length of the pipe. This then allows the control signals to filter down a pipeline and the Error condition to filter back up to the pipe controller.

SubSystem Signals

The SubSystem port on the board allows any transputer to control additional side pipes. A set-up like this allows for the generation of binary tree networks where the root has ultimate control over the network. Branches have the ability to Reset, Analyse and monitor the Error status of their daughter branches without affecting the rest of the network.

All the signals in the UpNot-, DownNot- and SubSystem- control networks are active low signals. This means that when there is a signal level of 0 Volts on the lines then the logic on the board will consider them to be in a TRUE condition.

Chapter 8. Outside World Interface

The SMT103 is a variation on an earlier board produced by Sundance, the SMT101. This earlier board had standard link connections, which unfortunately had a limited range. To overcome this problem the SMT103 has differential drivers on the link connectors on the edge connector. These provide far greater noise immunity over longer distances. According to Inmos data sheet 18 [1], the standard Inmos link has a theoretical maximum distance of 30cms. In practice however the distances that can be achieved using simple cabling methods is greater than this, Using the differential drive method then it is possible to achieve connection lengths of over 100 metres. It should be noted though that the RS422 specification places limitations on the transmission speed over certain lengths. At 5 Mbits/sec the length should be less than 25 metres and at 10 Mbits/sec it should be less than 15 metres. It should be noted though that the specification is deliberately conservative in its estimates.

Due to the complexity of the link options on this board Appendix C gives a schematic detail of the various Jumper connectons for the differential links. This is in the hope that it will clarify the details given in the rest of the manual.

Spare TRAM Links

Due to the space constraint on the back panel, some of the Links from the TRAM slots had to be omitted from the connector. These extra links are accessible, but you will have to make cables to connect to them. The following table (9) gives the link allocations.

Connector	Link number
JT01	TRAM 0 Link 0
JT03	TRAM 0 Link 3
JT13	TRAM 1 Link 3
JT23	TRAM 2 Link 3
JT33	TRAM 3 Link 3
PT	TRAM 3 Link 2

Table 9. Spare link connector allocation

For connectors JT01, JT03, JT13, JT23, and JT33 the LinkIn signal is connected to pin 2, and the LinkOut signal is connected to pin 1. Connector PT is the reverse of this in that LinkIn is on pin 1 and LinkOut is on pin 2. For connectors JT01, JT03, JT13, and PT pin 1 is the end of the strip nearest the DB37 connector. For connectors JT23 and JT33 pin 2 is the end of the strip nearest the DB37 connector.

Differential Links

To try and allow for maximum flexibility when connecting the differential link drivers some jumper links have had to be incorporated onto the board. At first the amount may seem quite daunting. On further investigation, you will see that they form common blocks, and once you have learned the setup for one link, then the others will be quite easy. However, the setup for DLink0 is different from the others in that it also has the ability to be connected to either of the C011's. The main reason behind all of these links is that in one mode the pinout on the back edge connector is compatible with that on boards made by CSA.

DLink 0

This is the most complicated of the links to explain. Not only does it allow for connection to the C011's, but it can also be connection to some of the internal link connected going to TRAMs and the onboard transputer.

JF1 and JF2 select whether the transmitter is connected to Link 1 of the transputer or another block of jumpers that further decide the link source. They must both be moved together, otherwise the link will fail to function.

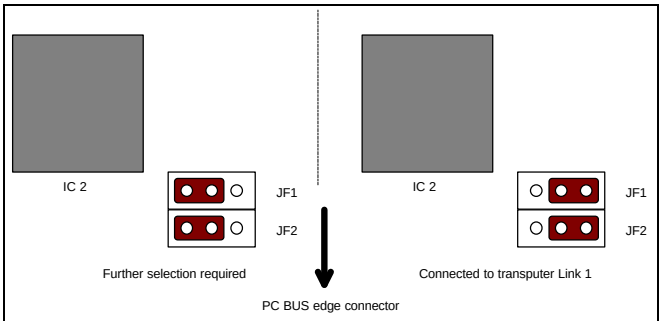


Figure 8. Differential link connections

If the "further selection" option is selected then another set of jumpers has to be setup so that the correct link option is used. You will have to note that only the valid options are described in this manual. There are ones that are not described, and if selected they may well cause the board to not work, or to damage some internal components.

DLinks 1, 2 and 3

The options for these links are far easier to select. The functionality is common between all three links, so once one has been described the others are fairly easy to implement. Basically there are only two different types of connections. The differential driver can be either connected to one of the links from the transputer, or to link 0 from one of the TRAM slots. It is a little more complicated than that though because the transputer link can be varied.

Jumpers JF3, JF4, JF5, JF6, JF7 and JF8 select whether the differential link is connected to either the transputer link or to the link selected by the next jumper blocks. Again there is an odd one out as DLink 3 can only be connected to transputer link 0 if J4, J5, J16 and J17 are set correctly. See later.

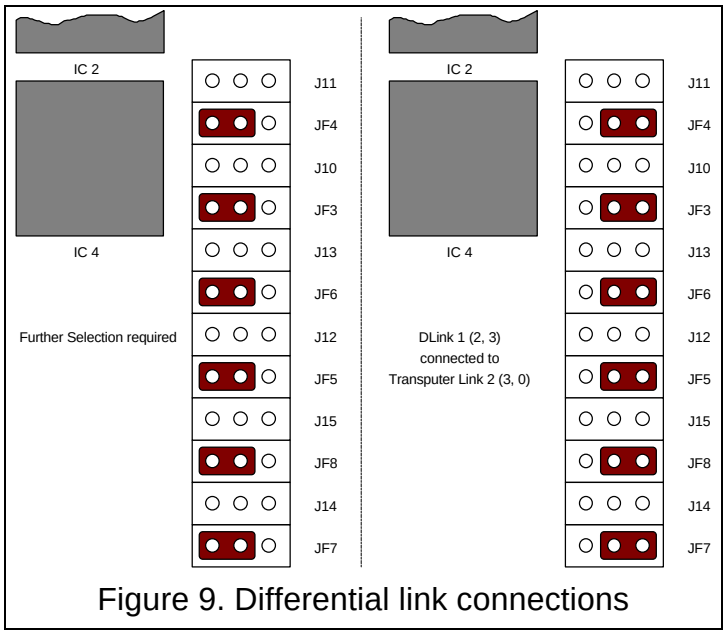


Figure 9. Differential link connections

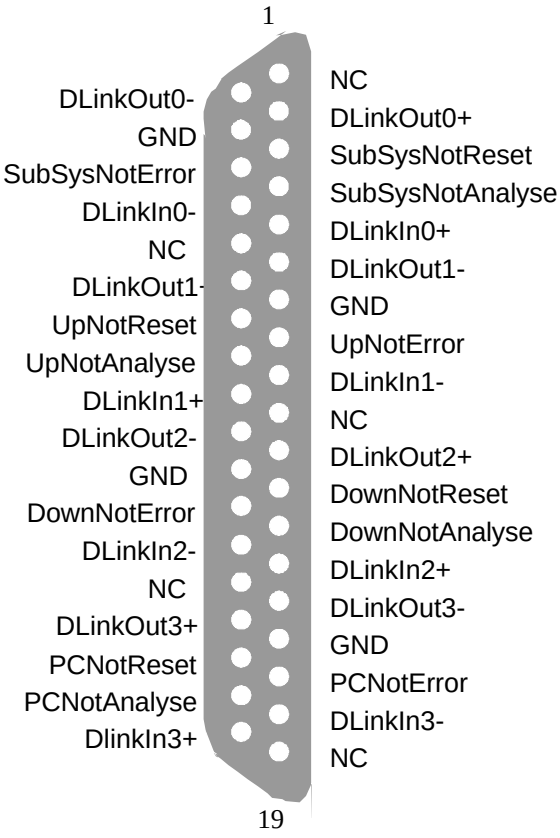
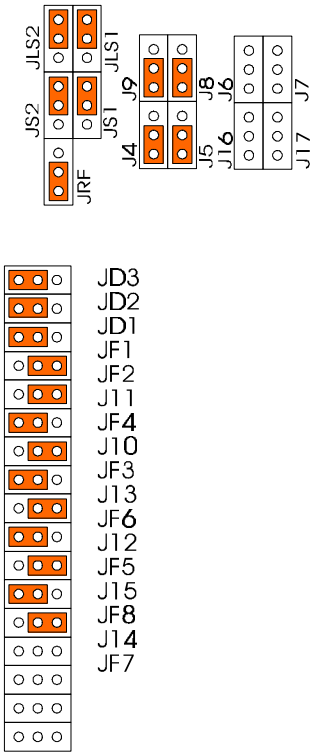


Figure 10. DB37 Connector pinout
(View looking into the connector)

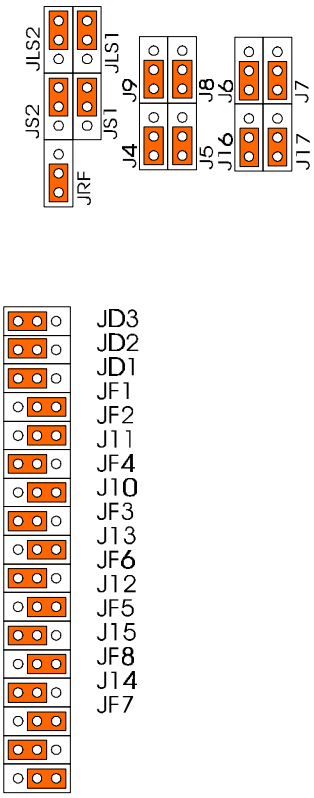
Appendix A

Example 1



In this option the first C011, that is the one decoded at #150, is connected to Link 0 of the onboard transputer. Link 1 of the transputer is connected to Differential link 1, Link 2 is connected to differential link 2 and link 3 is connected to differential link 3. Differential link 0 is not connected to anything. The RESET, ANALYSE and ERROR signals for the transputer are driven from the PCNot signals.

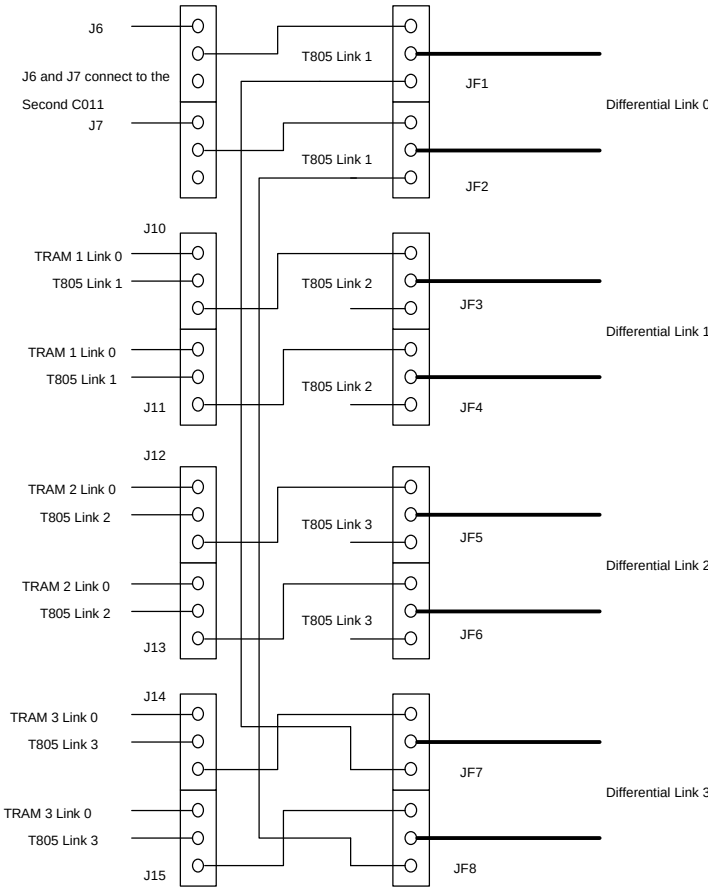
Example 2



The options in this example are the same as in the first with the added connection. Now DLink 0 is connected to the output from the second C011.

Appendix B.

To help explain the Jumper links here is a section of the schematic dealing with the differential links.



Appendix C. Errors on Issue 2 Boards

Due to an error with the layout of the Issue 2 PCBS there are several wires fitted to the board when it is shipped from Sundance. These modifications are relevant to all boards marked **ISSUE 2A**. These boards are also marked on the rear silkscreen as being copyright 1993.

The error is to do with the way in which the transputer link interface is connected to the differential drivers. The board was designed so that there was the option of either connecting the transputer links to the TRAM slots, or the external differential interface. Unfortunately some of the wires were crossed during the layout process. The final outcome of this is that if you use the jumper links to connect the TRAM slots to the transputer you in fact connect linkin to linkin and linkout to linkout. Not only will this not work, but it could damage the transputer linkout drivers.

To get around the problem you will find several wire links on the back of the board. These are set so that the default condition is to connect the links from the transputer to the TRAM slots

Transputer link	Default connection
Link 0	Not affected by these wire links
Link 1	Connected to TRAM slot 1, Link 0
Link 2	Connected to TRAM slot 2, Link 0
Link 3	Connected to TRAM slot 3, Link 0

Table 10. Default conditions

If you wish to use the differential drivers on the board then these wire links should be used and the jumpers J10, 11, 12, 13, 14 and 15 should be configured following the instructions given earlier in this manual.

If you wish to reconnect the links to the TRAM slots then you will have to put these wire links back in place. The best way of doing this is to solder directly to the pins of the jumper block on the back of the board. Figure 11 shows how these links should be fitted. To minimise the damage to the board and surrounding components this work should be carried out at an anti-static workstation with a fine tipped soldering iron. If you have an queries please contact Sundance technical support and they will be pleased to help you.

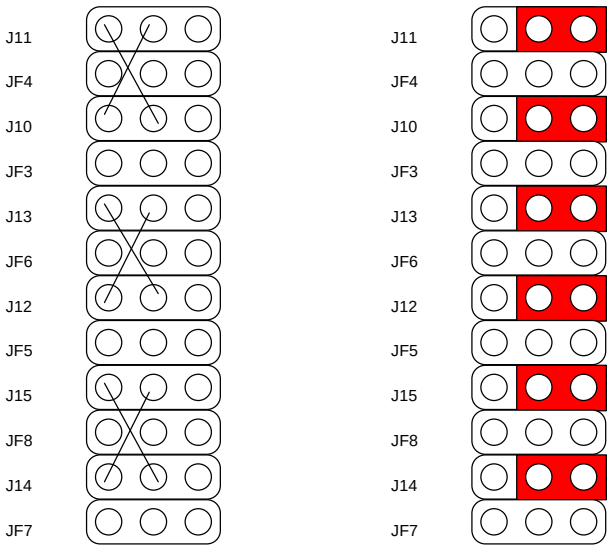


Figure 11. Modifications to link connections

Bibliography

[1] Trevor Watson and Michel Rygol, **INMOS Technical Note 18**; Connecting INMOS Links. INMOS, 1987

[2] Stephen Ghee, **INMOS Technical Note 11**; IMS B004 IBM PC add-in board, INMOS, 1987

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