HPT04

SCSI-2 TRAM

Purpose

This document covers the usage of the Glazier Systems Limited (GSL) HPT04 SCSI TRAM, both from an external hardware view, and from a progr ammer's view in sufficient detail to allow bespoke driver software to be developed if necessary.

GSL will normally supply the GSL SCSI Manager (CSM) and SCSI Device State Manager library (DSM) software with this TRAM, which we bashfully submit is the only interface you will ever need to our SCSI TRAM hardware. CSM and DSM are available for the most common Transputer programming environments, including 3L Parallel C, Inmos ANSI C and Occam Toolset. Software is documented separately.

Intended audience

By their very nature, TRAMs such as the HPT04 require some detailed knowledge of the Transputer and the TRAM standard in order to configure a working system. This level of expertise is assumed.

By and large, SCSI provides a relatively simple plug-and-play interface to high performance peripherals. However, SCSI still deals with devices at the raw block I/O level, and this is rightly regarded as he-man systems programmer's territory.

If a straightforward Transputer filesystem is all that is required, we recommend the GSL High Data Rate File System (for performance close to the raw block I/O rate), or the Helios® File Server (for Unix compatibility). Both are available for the HPT04, and both can interwork with CSM/DSM applications if necessary.

The SCSI port implemented by the HPT04 is a standard, single ended implementation, which should present no special problems. The programmer's information in this manual is intended to be read in conjunction with the appropriate T4/T8, NCR53C710 and SCSI documentation if direct programming of the hardware is contemplated.

Description

Physical

The HPT04 GSL SCSI-2 TRAM conforms to the dimensions and profile of the Size 2 TRAM layout defined in Inmos Technical Note 29, with the exception that vertical stacking is not possible in position 1 due to interference from the SCSI connector and associated components.

Dimensions:

Length:	92.96mm
Width:	53.33 mm
Height:	10.50 mm (above PCB, including SCSI connector)

Electrical

Power supply:

Voltage:	5.0V dc +/- 5%

Power dissipation:

20MHz processor:	2.4W
25MHz processor:	2.5W

SCSI bus

Single-ended connection

Optional parity

Synchronous transfer: 10Mbytes/second, req/ack offset 8

Optional fused terminator power

Socketed terminators

Active terminator option

10kV ESD protection

Configurable SCSI ID

Device complement

T400/T425/T805 32 bit Transputer /(20/25 MHz clock)

32MHz or 40MHz SCSI timing clock

NCR 53C710 32 bit DMA SCSI processor

4Mbytes DRAM

SCSI bus installation

Device ID

Controllers on a SCSI bus are distinguished by a unique device address, normally referred to as the SCSI ID. The SCSI ID is a number in the range 0-7. Controllers that respond to commands and manage devices are called targets, and controllers that issue commands to targets are called initiators. The vast majority of SCSI bus implementations have one initiator and one or more targets, although multi-initiator, multi-target configurations are possible. It is even possible for a single controller to respond as both an initiator and a target.

Each target controller can control up to eight physical devices, called logical units. The logical units are also numbered 0-7, giving rise to the term Logical Unit Number or LUN. Commonly, SCSI target controllers are integrated with the drive electronics, so it's not unusual to find all the devices occupying LUN 0 on their respective controllers, and only the SCSI IDs differ. Since there is normally one dedicated initiator (such as the HPT04) in the system to issue SCSI bus commands, a single SCSI bus can normally address seven target devices.

Although SCSI IDs are largely arbitrary, it is useful to adopt a convention when planning a SCSI bus to avoid unexpected clashes as devices are added. Setting the initiator SCSI id to 7 is a common convention, with the target devices allocated from 0 upwards. The SCSI ID of the HPT04 is normally set using jumpers J1, J2 and J3, although the jumpers actually set bits in a register to be read by the control firmware and loaded into the controller at boot time. The SCSI id set on the jumpers can of course be ignored o r overridden, if required.

When there are several devices contending for access on the bus, it should be noted that arbitration of the bus gives priority to higher SCSI IDs. Careful choice of SCSI IDs with reference to likely behaviour and access patterns will improve performance in these cases.

The location of the SCSI ID jumpers on the HPT04 is shown in Figure 1.

Figure 1 HPT04 SCSI-2 TRAM Jumper Layout

Termination

The SCSI bus, in the single-ended version implemented by the HPT04, is a bus with TTL-like signal levels, terminated by resistor networks at either end. The terminators are normally installed in the controllers at each end of the

bus. Since a particular controller (initiator or target) may or may not be at the end, it is common to provide the terminator resistor networks in sockets on each controller. Once the physical layout and SCSI bus cable path is determined, the terminators should be removed from all except the two end controllers.

On small, inter-cabinet installations (such as Sun Sparcstations), each device is supplied with an “in” and an “out” port, and the cabling is “daisy chained” from device to device (including the initiator in the workstation). This automatically leaves the two end out ports free for the installation of terminator stubs.

Another consideration is terminator power. Again, most controllers offer optional supply of terminator power to the bus via a jumper setting. A common convention is to allow the initiator to provide terminator power, since that controller is least likely to be removed from the system leaving the terminator network accidentally unpowered. In a well populated SCSI bus, it may be better electrically to have the terminator power provided by a controller in the middle of the cable to minimise the effects of cable length whether or not this is the initiator.

The HPT04 has socketed terminators and various terminator power options controlled by jumpers J4 and J5 (see Figure 1).

Device selection and performance

Unfortunately, what should be a simple scheme is complicated by the fact that some devices with integrated controllers do not have removable terminators, SCSI id jumpers or selectable terminator power. Controllers that commonly create problems in this area are initiators on small systems (such as Apple Macintosh or desktop Sparcstation) and systems that assume they will be the only target (some CD-ROMs and document scanners).

No matter what the device type, there are two important figures that gover n achievable data transfer rates. One is the continuous transfer rate, which on a disk or tape drive would correspond to the rate at which data bytes are read from or written to the media. The other is the actual bus transfer rate, sometimes referred to as the burst transfer rate. This is an important figure in high performance, multi-device systems, since combined with the continuous rate it gives an indication of bus occupancy. Several devices of a given continuous transfer rate can be shared efficiently on a single bus if their burst rates are high.

In most circumstances, devices on a SCSI bus do not interact significantly. One exception to this is when fast and slow devices are mixed on the same bus. Devices of low data transfer rate can occupy the bus for disproportionately long periods. Devices that incur long pauses during

transfer (such as floppy disks or tapes) can be particularly troublesome if the SCSI Disconnect feature is not supported.

In some circumstances, it may be worth considering the use of two or more separate SCSI controllers. Even though the devices could all be addressed on a single bus, devices with fixed terminators or fixed SCSI addresses can make some combinations impossible.

If the driver software is carefully constructed, the application-level consequences of operating 2 or more SCSI TRAMs can be minimised. Needless to say, the GSL support software is so constructed!

Cable recommendations

The original SCSI specification defined the single-ended bus for connections within a cabinet, and the differential bus for inter-cabinet connections. Most modern SCSI implementations cover a desktop at most, so the within-cabinet, single-ended specification is adequate. The differential bus specification is rarely used.

A simple, multi-drop SCSI cable can be constructed with 50-way IDC connectors and unshielded ribbon cable. This is perfectly adequate for short distances (say, up to 2 metres) within a piece of equipment. For separate, free-standing devices, a shielded cable with 50-way Cannon or Centronics connectors is preferred. Maximum total cable length is then about 6 metres. Refer to the SCSI/SCSI-2 specification for details on further detailed cable recommendations.

When connecting to the HPT04 itself, avoid too much downward pressure on the SCSI connector (and hence on the PCB). The PCB is stiff enough to take a reasonable amount of force, but the large VLSI devices can be susceptible to lead fractures if too much force is applied.

TRAM installation

The HPT01 is a standard, Size 2 TRAM with subsystem control. It is compatible with most TRAM motherboards such as the Inmos B008. It respon ds to the LinkSpeed and Reset/Analyse pins as specified in Inmos Technical Note 29. Extended Link speed options are available as detailed in Table 1.

Link_Speed_A	0.00	1.00	0.00	1.00
Link_Speed_B	0.00	0.00	1.00	1.00
Selected Speed (MHz)	10.00	N/A	N/A	20.00

Table 1 Extended LinkSpeed Options

Note that where high transfer rates into an application on a separate processor are required, the link bandwidth can be a limiting factor. Although

the HPT04 is uncommitted in its link usage, we recommend at least two links operating at 20Mbits/sec. be configured for transfer of SCSI device data.

The application-level programming consequences of aggregating 2 or more links together can be hidden by a suitable transport protocol, such as GSL's TDP. The GSL SCSI Manager library uses TDP to manage this aspect.

A standard Size 1 TRAM can be stacked vertically in position 2 on this TRAM. In situations where this TRAM will be the boot device, we recommend the GSL HPT21 Flash EEPROM TRAM or HPT20 EPROM TRAM in this position. The extended feature pins in position 2 will allow the HPT04 to be booted whilst presenting all links to the motherboard as uncommitted once the boot image is transferred.

Figure 3 NCR 53C710 Memory

FFFFFF16 Unassigned

20000016 1FFFFF16 4096kbytes RAM

00000016

FFFFFFFF16 Unassigned

8020000016801FFFFF16 4092kbytes external RAM

8000100016 80000FFF16 4kbytes internal RAM (T425/T805 shown)

80000000167FFFFFFF16 Unassigned

6000010016600000FF16 LSB read/write of 53C710 byte lane registers (see text)

3000000016

2FFFFFFF16 Unassigned

2000010016 - 200000FF16 Word read/write of 53C710 registers

2000000016 - 1FFFFFFF16 Unassigned

0000000816

0000000416 Write: bit 0 = SubSystem Analyse

0000000016 Write: bit 0 = SubSystem Reset Read

Read bit 0 = SubSystem NotError

bit 1 = SCSI ID bit 0 (J1)

bit 2 = SCSI ID bit 1 (J2)

bit 3 = SCSI ID bit 2 (J3)

(jumper present = 0)

Figure 2 Transputer Memory Map

Programming modeL

The HPT04 is available with comprehensive drivers for most common languages and environments, including 3L Parallel C, Inmos ANSI C, Occam Toolset and Helios. Whilst these should solve most problems without recourse to device-level programming, the following provides additional low-level information should the need arise.

Transputer memory map

The Transputer hardware cannot generate a byte read. Nevertheless, some 53C710 registers must be read in byte mode to avoid loss of interrupt context information. In addition to the complete register map at 2000000016, the registers are mapped into memory starting at 3000000016, 4000000016, 5000000016 & 6000000016 in such a way that only the byte lane 3, 0, 1 & 2 respectively is active, even though the Transputer may issue a word read/write.

For further information on the registers of the SCSI device used, refer to the NCR 53C710 Programmer's guide and Data manual.

SIOP memory map

The SCSI I/O processor fitted is an NCR 53C710. It contains a 32 bit RISC processor and master mode DMA engine. The device is normally operated by placing entire SCSI transfer machine code routines into memory, an d manipulating the 53C700 registers to execute the code.

The top seven bits of the 53C710 address bus is not decoded, so although the entire memory space wraps at 4Mbytes, the Transputer's addresses can generally be used in 53C710 instructions without change. For software compatibility with future upgrades to this TRAM, we recommend you do not make use of this "wraparound" effect.

Note that addresses from 8000000016 to 80000FFF16 (800007FF16 on the T400) represent internal RAM to the Transputer, but external RAM to the 53C710. If the 53C710 is set to perform DMA to/from this address range, it will not access internal memory the Transputer sees mapped in these addresses.

Interrupts

The 53C710 interrupt line is connected to the Event handshake on the T801. A 53C710 interrupt appears as a single word on the Event channel. Interrupt acknowledge is achieved by reading the appropriate ISTAT/DSTAT/SSTAT register.

HPT04-Specifics

The hardware implementation of the SCSI TRAM using the 53C710 has certain consequences for register-level programming of the device. These are as follows:

Clock frequency

The BCLK input to the 53C700 is the ProcClockOut signal from the Transputer. This may be 20 or 25MHz. This is used to derive host bus-related signals only, so its frequence is transparent to software.

The SCLK input is generated by a 32MHz or 40MHz crystal. The correct value must be used to program DCNTL CF1/CF0 and SBCL SSCF1/ SSCF0 to the correct divide ratio for SCSI bus timing. As it happens, CF1/CF0 will be 1/0 in both cases. Also, the values programmed into SXFER TP2/ TP1/ TP0 as a result of synchronous transfer negotiation depend on this frequency.

Parity

The 53C710 can use parity bits in host memory rather than generating parity internally. However, the HPT04 does not implement parity memory, so this feature should not be programmed. SCNTL0 EPG should be 1 to force parity generation on output to the SCSI bus (whether or not the device being addressed supports parity). For parity checking on input, SCNTL1 EPC can be 1 or 0 as required.

Differential mode

The HPT04 has no support for differential mode SCSI, so CTEST7 DIFF should be 0.

Extra cycle of data setup

The HPT04 does not require the extra cycle of data setup time, so SCNTL1 EXC should be 0.

DMA block length

The HPT04 memory bandwidth is sufficiently high that DMA block lengths do not need to be restricted. DMODE block length parameters should be set to allow 8 word transfers.

User programmable bits

The FC2/1/0 and TT0 bits are unconnected, so DMODE FC2/1, PD, TT0 and CTEST8 FM are unused.

Enable Ack

STERM assertion is not expected byt the HPT04 control logic, so DCNTL EA should be 0.

Multiplexed address/data

The HPT04 runs the 53C710 in multiplexed address/data mode, so CTEST4 MUX should be 1.

Cache/burst mode

The HPT04 has no cache/burst support, so CTEST7 CDIS should be set to 1.

Snoop pins and transfer type

The HPT04 implementation makes no use of the snoop control function, so CTEST7 SC1/SC0/TT1 and CTEST8 SM are unused.

Fast arbitration

The HPT04 arbitration logic is not designed to support fast arbitration mode, so DCNTL FA should be 0.

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