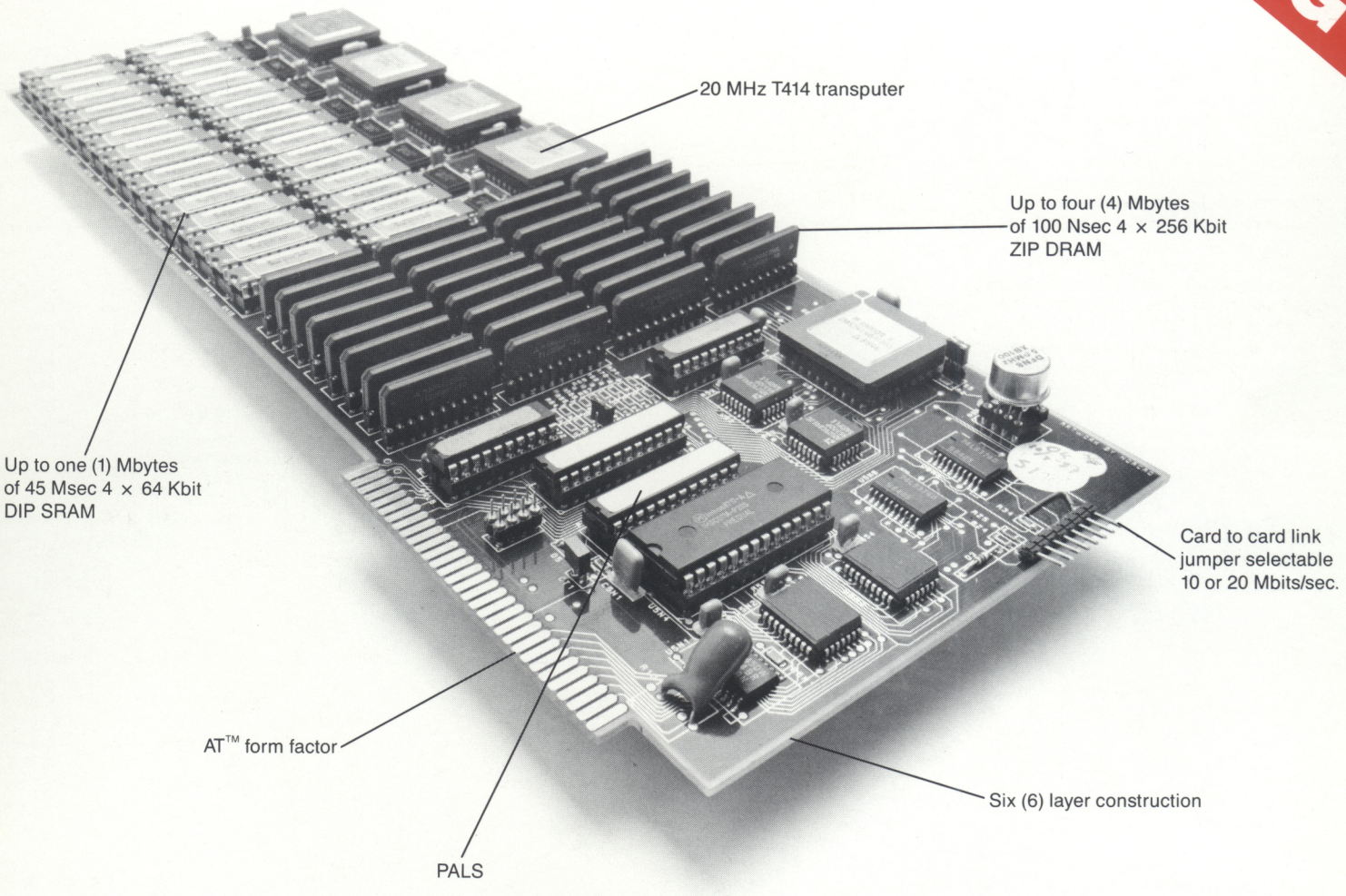
INTRODUCING

- Up to 50 MIPS performance per card
- Multiple cards per PC
- Raster Imaging software available
- Matched graphics card available



The Leonardo™ Series

High preformance parallel coprocessor card from

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THE LEONARDO™ SERIES

The Leonardo™ is an AT™ compatible single board high performance parallel coprocessor that is populated with up to five (5) IMS T414 (transputer) 32-bit microprocessors, providing execution of up to 50 MIPS. The transputers are arranged in a "Master and Slaves" pipe that can be expanded over multiple cards, extending performance beyond 50 MIPS. Each master is configured with up to four (4) megabytes of RAM and each slave is configured with 256 Kbytes of RAM. Both microprocessors and memory are socketed. Transputers are programmable in "C," Fortran or Pascal, but optimal results are achieved using Occam, the native high level programming language that provides true parallel processing.

CARD SPECIFICATIONS

Microprocessor

One (1) or more INMOS IMS T414-20 transputer (Option: T800) 32-bit microprocessors, operating at 20 MHz, each with four (4) standard transputer communications links, 2K bytes of on-chip SRAM, memory and peripheral interfaces. Procedure calls, process switching and interrupt latency are sub-microsecond, with microcode support for floating point operations. The T414 uses a 32 bit wide memory interface with multiplexed data and address lines to provide a data rate of up to 4 bytes every 150 nano seconds (26.6 Mbytes/sec) and can directly address up to four (4) Gbytes. The onboard SRAM provides a maximum data rate of 80 Mbytes/sec. The transputer uses a DMA block transfer mechanism to concurrently transfer messages between memory and other transputers via the links. The optional T800 operates at 20 MHz, and contains an on-chip 64-bit microcoded floating point unit able to support single length (32-bit) and double length (64-bit) arithmetic according to the ANSI/IEEE 754-1985 standard. Floating point operations may execute concurrently with CPU operations.

Physical dimensions

H – 33.8 cm, including link connector
V – 12.9 cm, including mother board connector.
Weight – app. 475 g.

Environmental specifications

Relative humidity: 40–80% (non-condensing)
Temperature: 10–40 degrees C

Power consumption

SRAM version: 36 watts, peak, 7.5 watts, continuous
DRAM version: 32 watts, peak, 8.0 watts, continuous

Memory

Master transputer: up to four (4) MBytes of socketed 100 nanosecond 4 × 256 Kbit ZIP components.

Slave transputers: 256 KBytes of socketed 45 nanosecond 4 × 64 Kbit DIP SRAM components (150 microsecond bus cycle) per slave (maximum per card of one (1) MByte). Or up to 256 Kbytes of socketed 100 nanosecond 4 × 64 Kbit ZIP DRAM (250 microsecond bus cycle) per slave (maximum per card of one (1) MByte).
A 26.6 MByte/sec data rate is achieved between off-chip memory and the transputer.

Form factor

AT™

Software

(available from Inmos and other sources)
"C" compiler
Pascal compiler
Fortran compiler
Occam compiler – native concurrent (parallel) programming language
TDS (transputer Development System) – Occam development environment, with various libraries and tools
PABLO – SimTech proprietary raster to vector encoding and decoding language for scanned graphics

Links, internal transputer to transputer

Each transputer has four (4) links and when connected in a pipe (see illustration) uses two (2) links to connect to each of its neighbors, leaving two links free on each end for external connection. Using these links, a maximum data rate of 6.4 MBytes/sec is achieved between on-chip memory and the link.

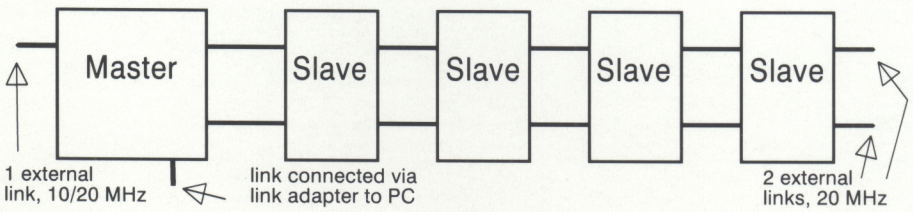
Links, external

Three (3) transputer to external device links are provided, two with a 20 Mbit/sec transfer rate and one with a jumper selectable rate of either 10 Mbit or 20 Mbit/sec.

Links, PC

The master transputer is connected to the host PC via a standard Inmos link adapter. The link adapter is extended with 2K of dual-ported 45 nanosecond SRAM. This PC connection provides a transfer rate of up to 800 KBytes/second when using the OUTSTR and INSTR instructions on the PC's 80286 CPU. Optional interrupts are available by jumper selection.

The Pipe



Microprocessor benchmarks

T414 (20 MHz) – 663 KWhetstones/sec on single length arithmetic. 50nS internal cycle time. 10 MIPS.
T800 (20 MHz) – 4 MWhetstones/sec on single length arithmetic. 50nS internal cycle time. 10 MIPS. 1.5 MFLOPS, 32-bit single precision, 1.1 MFLOPS, 64-bit double precision.

Typical floating point arithmetic operation times

		IMS T414–20 MHz	IMS T800–20 MHz
REAL 32			
	+, –	11.5 microS	350 nanoS
	*	10.0 microS	550 nanoS
	/	11.3 microS	800 nanoS
REAL64			
	+, –	28.2 microS	350 nanoS
	*	38.0 microS	1000 nanoS
	/	55.8 microS	1550 nanoS

Sieve benchmarks, processor comparison

device	Language	msec
IBM PC/XT	Fortran	2,370
IBM XT/370	Fortran	1,300
PDP 11/34	Fortran	800
APOLLO DN/300	Fortran	450
IBM 4331-2	PL/1	350
68000, 8 MHz	Assembler	155
VAX 11/780	Fortran	150
VAX 11/785	Fortran	90
68020, 16.7 MHz	Assembler	58
T414, 20 MHz	Occam	42
IBM 3081 K	Fortran	8

All specifications subject to change without notice.
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