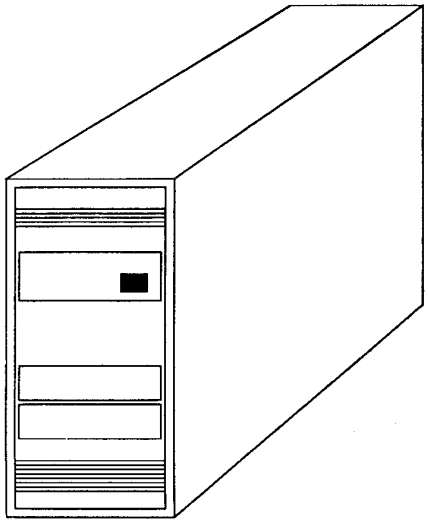
Computer System Architects
100 Library Plaza
15 North 100 East
Provo, Utah 84606-3100

PART.E4

4 Slots with 100 watt Power Supply

Expansion Chassis

(with PC/AT-size card slots)



Features

- Accommodates 4 full-length PC/AT-size circuit boards on 0.8 inch centers
- 100 watt switching power supply
- 110/220 VAC switchable input
- Table-top enclosure
- Epoxy painted enclosure (off-white)
- Three 3.5" disk slots (two with front panel bezels)
- Lighted power switch
- Reset switch (optional)
- 1.5" speaker (use optional)
- Ideal enclosure for all CSA board-level transputer products (except for the PART.8 VME-bus interface)
- Ideal for inclusion within the same chassis of a single-board 80286 or 80386 host processor (optional)

Description

The PART.E4 expansion chassis delivers high quality power and cooling to up to 4 PC/AT-size circuit boards. Power is evenly distributed to all slots, and the power supply fan provides ample air throughout.

The PART.E4 is ideal for housing CSA transputer boards and accessories. Transputers can be interconnected with each other within the same cabinet, with transputers within other cabinets, or with an external host computer having a link interface.

A single-board computer can accompany the transputers within the same PART.E4 enclosure, providing a powerful, yet exceptionally compact and economical, solution.

The CSA PART.E4 is delivered complete with power cord and one year warranty.

Power Requirements

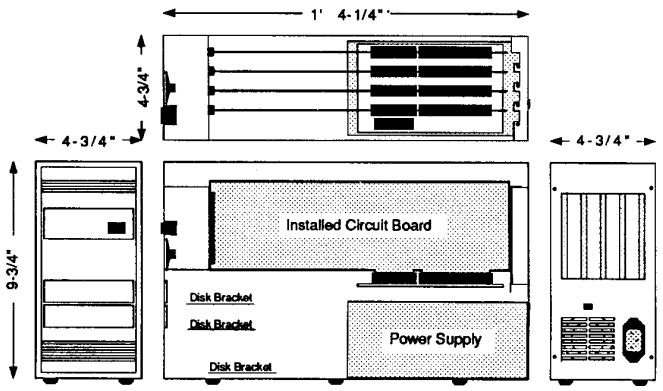
PART.E4: 1.9 Amps @ 90-132 VAC; 47-63 Hz
1.0 Amps @ 180-264 VAC; 47-63 Hz

Output voltages

+5 VDC at 12 Amps, - 5 VDC at 0.3 Amp,
+12 VDC at 8 Amps, - 12 VDC at 0.3 Amps.

Cooling

One 2" fan in power supply.



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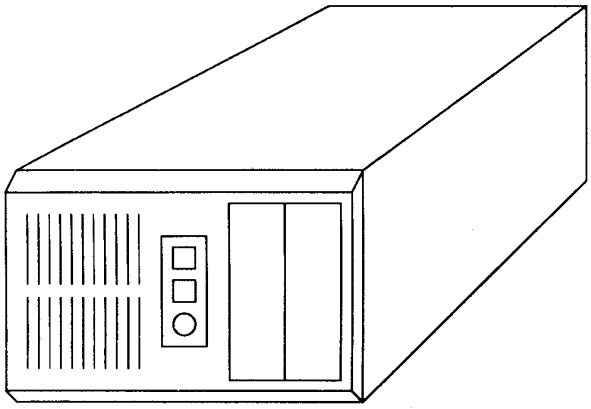
PART.E6

6 Slots with 200 watt Power Supply

Expansion Chassis

(with PC/AT-size card slots)



Features

- Accommodates 6 full-length PC/AT-size circuit boards on 0.8 inch centers
- 200 watt switching power supply
- 110/220 VAC switchable input
- Table-top enclosure
- Epoxy painted enclosure (off-white)
- One full-size vertical 5.25" disk slot
- Washable air filter on front bezel
- Lighted power switch
- Reset switch (use optional)
- Ideal enclosure for all CSA board-level transputer products (except for the PART.8 VME-bus interface)
- Ideal for inclusion within the same chassis of a single-board 80286 or 80386 host processor (optional)
- Chassis carries full agency approvals

Description

The PART.E6 expansion chassis delivers high quality power and cooling to as many as 6 PC/AT-size circuit boards. Power is evenly distributed to all slots, and the fan plenum provides ample air throughout.

The PART.E6 is ideal for housing CSA transputer boards and accessories. Transputers can be interconnected with each other within the same cabinet, with transputers within other cabinets, or with an external host computer having a link interface.

A single-board computer, along with various non-transputer PC add-in boards can accompany the transputers within the same PART.E6 expansion chassis, providing a powerful, yet compact, solution.

The CSA PART.E3 is delivered complete with documentation, power cord, and one year manufacturers warranty.

Power Requirements

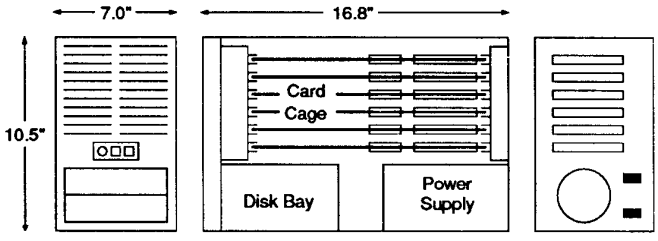
PART.E6: 3.5 Amps @ 90-132 VAC; 47-63 Hz
1.7 Amps @ 180-264 VAC; 47-63 Hz

Output voltages

+5 VDC at 18 Amps, - 5 VDC at 1.0 Amp,
+12 VDC at 5.0 Amps, - 12 VDC at 0.5 Amps.

Cooling

One 52 cfm fan (12V at 0.12A) housed in plenum directed across all 6 card slots. Also, one 2" fan in power supply.



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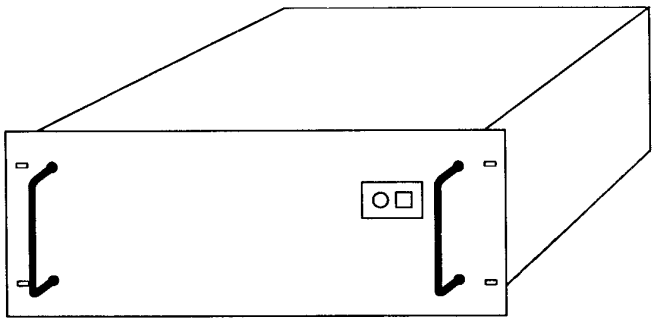
PART.E20

20 Slots with 400 watt Power Supply

Expansion Chassis

(with PC/AT-size card slots)



Description

The PART.E20 expansion chassis delivers high quality power and cooling to as many as 20 PC/AT-size circuit boards. Multiple service entries evenly distribute power to all slots, and the multiple fan plenum provides ample air throughout.

The PART.E20 is ideal for housing CSA transputer boards and accessories. Transputers can be interconnected with each other within the same enclosure, with transputers within other enclosures, or with an external host computer having a link interface.

A single-board computer, along with various non-transputer PC add-in boards can accompany the transputers within the same PART.E20 expansion chassis, providing an extremely powerful single-box solution.

The CSA PART.E20 is delivered complete with documentation, power cord, and one year manufacturers warranty.

Features

- Accommodates 20 full-length PC/AT-size circuit boards on 0.8 inch centers
- 400 watt switching power supply (500 watt optional)
- 110/220 VAC switchable input
- Rack-mount enclosure (optional table-top)
- Black anodized brushed front panel with handles
- Captive rack mounting nuts installed for optional rack-mounting slides
- Lighted power switch
- Reset switch (use optional)
- Ideal enclosure for all CSA board-level transputer products (except for the PART.8 VME-bus interface)
- Ideal for inclusion within the same chassis of a single-board 80286 or 80386 host processor (optional)
- Chassis carries full agency approvals

Power Requirements

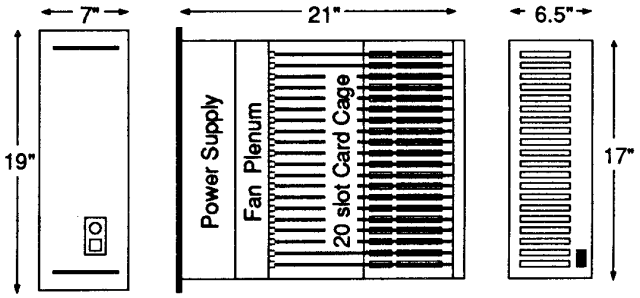
PART.E20: 6 Amps @ 90-132 VAC; 47-63 Hz
3 Amps @ 180-264 VAC; 47-63 Hz

Output voltages

+5 VDC @ 50 Amps, -5 VDC @ 1.0 Amp,
+12 VDC @ 7.0 Amps, -12 VDC @ 1.0 Amp.

Cooling

Three 33 cfm fans (12V @ 0.19A each) housed in plenum directed evenly across all 20 card slots.

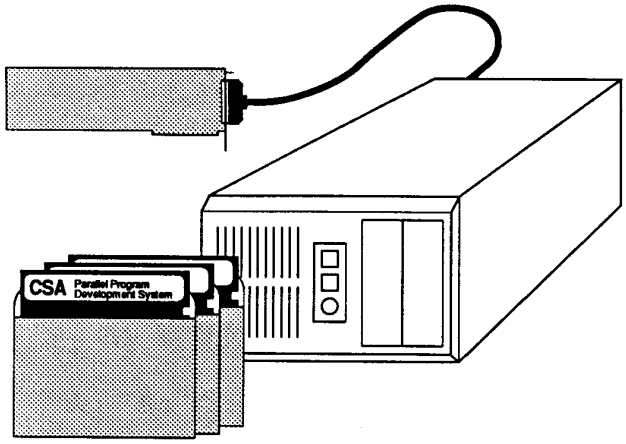


Computer System Architects
950 North University Avenue
Provo, Utah 84604-3422

SuperSet.16

For PC, Macintosh, or Sun Workstations

16-Node Hypercube Parallel Compute Engine



Features

- High Performance Parallel Compute Engine
  - Up to 255 MIPS
  - Up to 36 MFLOPS (with 30-MHz T805 option)
  - Up to 512 megabytes of RAM
- Parallel Architecture
  - Multiple instruction, multiple data stream (MIMD)
  - No shared memory; no shared memory bottleneck
  - High speed interprocessor message-passing links
- 16 Compute Nodes
  - 16 32-bit transputer processors
    IMS T425's, or
    IMS T805's (with on-chip floating-point)
  - Additional "root" node with host interface
  - Expandable
- Parallel Programming Tools
  - "C", FORTRAN, Modula-2, and Occam2 Compilers (with concurrency libraries)
  - Network configurers and loaders
  - Host servers under DOS and UNIX
- Choice of Host Environments
  - IBM PC, XT or AT (and compatibles) under DOS
  - SUN Workstations under UNIX (most models)
  - Macintosh

Description

The SuperSet.16 is a high performance parallel computing engine designed to operate in conjunction with a workstation host. It consists of a host interface add-in board and a small desk-top or rack-mountable cabinet housing 16 compute nodes (32-bit transputers, each with local RAM), a 17th system management "root" node (also a 32-bit transputer), and an interprocessor communication switch.

Each of the 17 transputer nodes is, by itself, a powerful processor, executing 10-15 million RISC-like instructions per second and directly addressing up to 32 megabytes of local memory. The transputer is unique among microprocessors in that it was explicitly designed to be a component processor within an array of processors. This is facilitated by a built-in hardware scheduler and the incorporation, on-chip, of 4 high-speed, bidirectional communication links which operate in the background (under DMA control) while processing continues. Utilizing this capability, a single processor can communicate with its neighboring processors at a rate of up to 9.2 million bytes per second; nearly half the bandwidth of a typical 32-bit memory bus.

In many SuperSet systems, the high-end T805 transputer model is used. The T805 has an on-chip floating-point coprocessor and yields up to 1.5 million 64-bit floating-point operations per second (1.5 MFLOPS), or 2.25 MFLOPS at 32 bits. These figures are based on an even mix of *scalar* adds, subtracts, multiplies, and divides.

The table below compares the performance of a single 20-MHz T805 processor with various other processors (using the LINPACK benchmark). No hand-optimization was allowed for these timings; just what could be obtained using FORTRAN compilers. The Cray-1S performance is used as the unit of measure, noting that a Cray-1S is (of course) capable of much greater performance if hand-optimization and optimal selection of vector lengths is allowed.

	64-bit		32-bit	
Processor Type	Ratio	MFLOPS	Ratio	MFLOPS
Cray -1S	1	12		
DEC VAX 8800	12	0.99	9	1.36
SUN-3/260 + FPA	27	0.46	14	0.86
T800 Transputer	33	0.37	29	0.43
DEC VAX 11/785 FPA	67	0.18	31	0.40
DEC microVAX II	97	0.13	70	0.17
SUN-3/260, 20MHz 68881	108	0.113	97	0.13
Apollo DN3000	197	0.062	174	0.068
IBM PC-AT, 80287	1341	0.009	891	0.013
Apple Macintosh	3196	0.004	1723	0.007

LINPACK benchmark code and performance figures supplied by Jack Dongarra of the Mathematics and Computer Science Division at Argonne National Laboratory.

In order to exploit the power of the SuperSet.16, the user explicitly provides for parallelism within his program. This is done by segmenting the problem, in time or space, such that a portion of it can be simultaneously worked upon by as many compute nodes as are available. Usually, rather course-grained tasks can be implemented in a quite normal fashion on each node, with concurrent processes being implemented to pass messages between the nodes as work progresses. In some situations all compute nodes may contain identical code, while in others each one's code might differ. In some cases the root node might be programmed to dynamically allocate compute node work load on a somewhat random, as-available basis. In other cases each node might be made to cooperate interactively with its nearest neighbors, iteratively passing messages back and forth as processing proceeds.

The nodes within the SuperSet.16 come interconnected as shown in the figure to the right. The topology is essentially that of a 4x4 2-dimensional mesh with wrap-around (which, by the way is equivalent to a 16-node torus and also to a 4-dimensional cube, or hypercube). The only deviation from this regular structure occurs at the upper edge of the mesh, where a link switch provides a pathway to the host (via the root node) or the ability to convert the mesh into a regularized pipeline. Using a proprietary signalling capability, the setting of the link switch can be dynamically controlled by the application program running in the upper-left compute node, allowing run-time switching between a pure hypercube structure and one that allows for host I/O.

A unique feature of the CSA SuperSet is that its interconnect topology can very easily be changed to any configuration desired by the user, within the basic limitations of the link switch and the transputer itself. All link interconnections are made by way of miniature, high-reliability, jumper cables. Link connections can also be made to other CSA devices which can be housed within the same or another chassis. (See data sheets for members of the CSA PARTS family.)

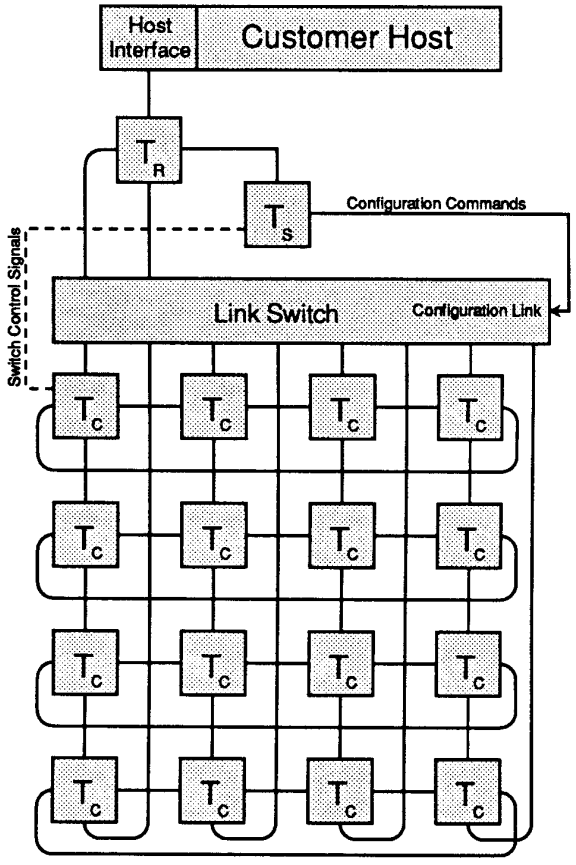
The SuperSet.16 can be programmed in "C", FORTRAN-77, Occam, Modula-2, or a combination of these. The "C," FORTRAN, and Modula-2 compilers come with special concurrency libraries, network loaders, etc. to facilitate parallel implementation. Occam is a special parallel processing language designed specifically for the transputer architecture. (Refer to CSA transputer software data sheets.)

Options

The CSA SuperSet.16 can be purchased in any of a number of configurations relative to processor model (T425 or T805), processor speed (20, 25, or 30 MHz), memory size (from 256K to 32M bytes per node) and memory speed (zero or one wait-state). Selecting from among these options, the customer can configure systems that perform practically anywhere within the low-end to high-end range shown in the following table.

	Low-End	High-End
Processors	20MHz T425's	30MHz T805's
RAM per compute node	256 K Bytes	8 M Bytes
RAM on root node	256 K Bytes	8 M Bytes
Total RAM	4.25 M Bytes	136 M Bytes
Total MIPS	170 MIPS	255 MIPS
Total FLOPS (64-bit)	1 MFLOPS	**24 MFLOPS**
Total FLOPS (32-bit)	2 MFLOPS	**36 MFLOPS**

Various configuration options for the SuperSet product line can be specified at the time of purchase by following the SuperSet systems part-numbering conventions included with copies of the CSA price list. Contact CSA directly for further information regarding the SuperSet.16, or for a quotation on a particular configuration.



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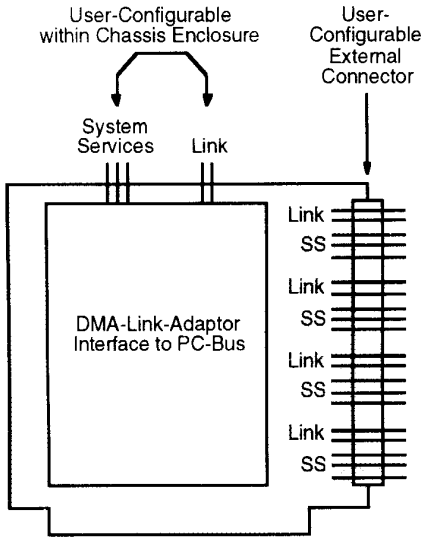
100 Library Plaza
15 North 100 East
Provo, Utah 84606-3100

PART.0 DMA-Link-Adaptor Interface for the PC Bus



Features

- 8-bit parallel interface to PC bus
  - Programmed I/O or DMA
  - PC interrupt capability
  - Data transfer at greater than 200K bytes/sec (up to 800K bytes/sec using blind read/write)
- Bidirectional serial transputer link
  - User configurable
  - Speed selectable to 20M bits/sec
  - Differentially buffered for greater reliability
- Programmable system services (reset, analyze, error)
  - Host can control transputer reset and analyze
  - Host can detect transputer error
- Plugs into a CSA chassis, or optionally into an IBM PC bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Compatible with Transputer Education Kit boards
- Compatible with Inmos evaluation boards

Description

CSA's PART.0 does not include a transputer. It is simply a parallel-to-serial/serial-to-parallel transputer link interface circuit on a half size card which can be plugged into an IBM PC, PC/XT or PC/AT. It can also be plugged into most PC compatibles as well as APOLLO workstations having an AT bus, and the Sun 386i.

The bidirectional serial transputer link is brought to connector pins on the upper edge of the circuit board such that connection can be made to transputers on other CSA PARTS boards within the same chassis. In addition, a 37-pin connector is provided on the rear edge of the board through which this link can be connected to CSA PARTS boards within other cabinets. The transputer link is differentially driven, providing reliability over distances in excess of 40 feet. The CSA PART.0 link circuitry is electrically terminated so that it is also possible to directly connect it to the single-ended drivers and receivers on the various Inmos evaluation boards, the CSA Transputer Education Kit and the products of several other manufacturers.

System services signals (transputer reset, analyze, and error) are available along the upper edge of the board along with the link. There are also system services pins provided on the external connector. All system services and link signals are thus user-configurable, making it possible for the PC or other host workstation, through the link adaptor, to act as a master to an arbitrarily large network of transputer processors.

The transputers on most CSA PARTS boards are configured to boot from link, and as such they can accept code down-loaded through the CSA PART.0 link adaptor. This code can be generated by any of the compilers provided by Inmos and most other software vendors, including CSA, Logical Systems, and 3L, Ltd.

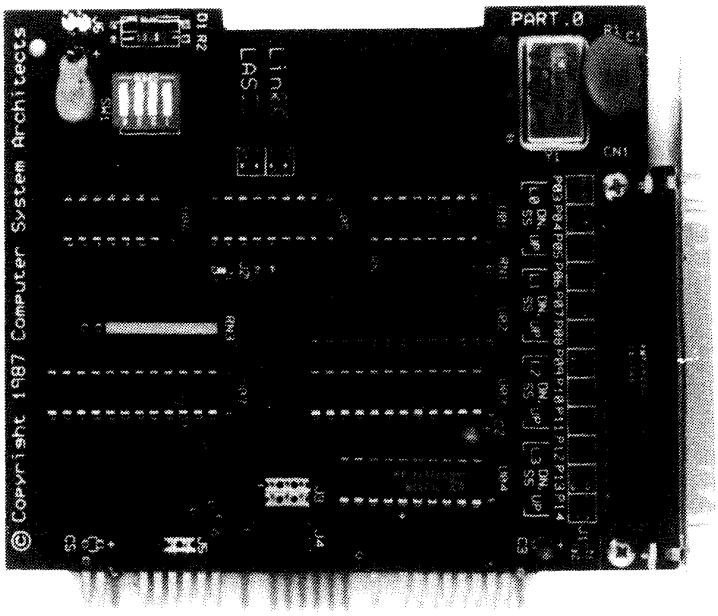
(all of which CSA distributes).

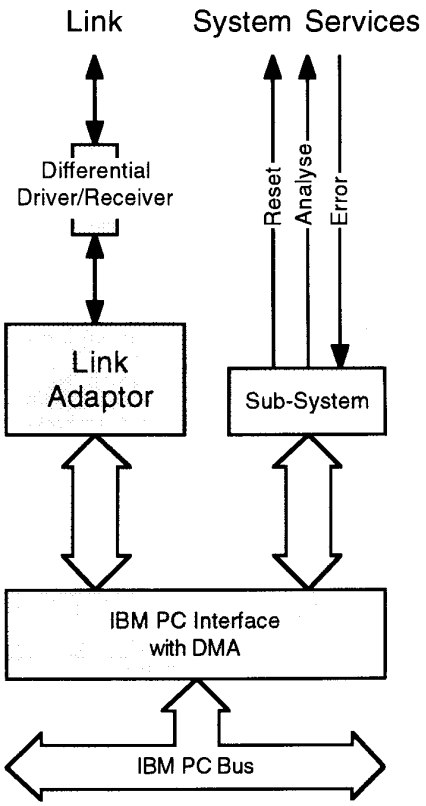
The PART.0 is delivered with :

1. 2 PART.C1 Internal Signal Cables for link and system services interconnection within the same enclosure.
2. Diagnostics and sample programs on floppy disk.
3. Documentation package.

Power Requirements

0.5 A @ 5.0 V (typical)





Link Adaptor Block Diagram

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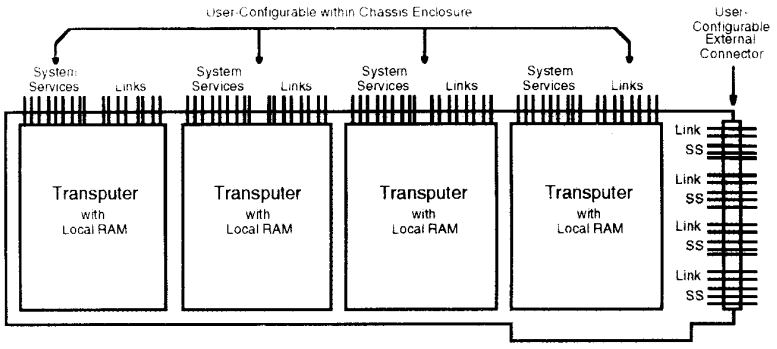
PART.1

with 256 KB of DRAM per processor

Multi-Transputer Board

(with 4 processors)



Features

- 4 Inmos 32-bit transputers
  - Accomodates the T400, T425 or floating point T805
  - Accomodates 20, 25, or 30 MHz transputers
- 256 KBytes of DRAM per transputer
- 16 bidirectional serial links (with 4 transputers)
  - 4 links from each transputer
  - 100% user configurable
  - Speed selectable to 20 Mbits/sec
  - Differentially buffered for greater reliability
- Plugs into a CSA chassis, or optionally into an IBM PC bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Compatible with Transputer Education Kit boards
- Compatible with Inmos evaluation boards

Description

CSA's PART.1 is a multiprocessor computing module consisting of one, two, three or four 32-bit transputers, each with 256 KBytes of local RAM.

All four links of each of the four transputers are brought to connector pins on the upper edge of the circuit board. The pins provide easy interconnection between processors on the same board or on other boards within the same enclosure. In addition, a connector is provided on the rear edge of the board through which up to four links can be connected to boards within other enclosures or cabinets.

All CSA links are differentially driven, guarantying reliable interconnection of devices over distances of 40 feet or more. Furthermore, CSA link signals are electrically terminated so that they can also be directly connected to raw TTL drivers and receivers as implemented on Inmos and other manufacturers' boards.

In addition to functioning as a transputer with local RAM, each of the four processor nodes is capable of providing system services (i.e. of generating reset and analyze and of sensing error) via memory-mapped I/O circuitry. Thus any node can act as master to other nodes to which it might be interconnected.

System services signals for each of the four transputers are available along the upper edge of the board along with the links. There are also four sets of user-configurable system services pins provided on the external connector. Thus each of the transputers can be configured to act as a master or as a daisy-chained slave within an arbitrarily large network of processors.

PART.1 boards can be plugged into spare IBM PC card slots (they are not logically interfaced to the PC) or into an external desk-top or rack-mounted enclosure (see the PART.E4, PART.E6 or PART.E20). A logical interface to a host processor can be made via link interconnection through a CSA DMA-Link-Adaptor circuit as provided on various CSA boards (e.g. the PART.0, PART.4, PART.5, PART.8, or TEK.1).

The transputers on the PART.1 board are configured to boot from link, and will accept code as generated by Inmos and most other vendors' program development systems.

Options

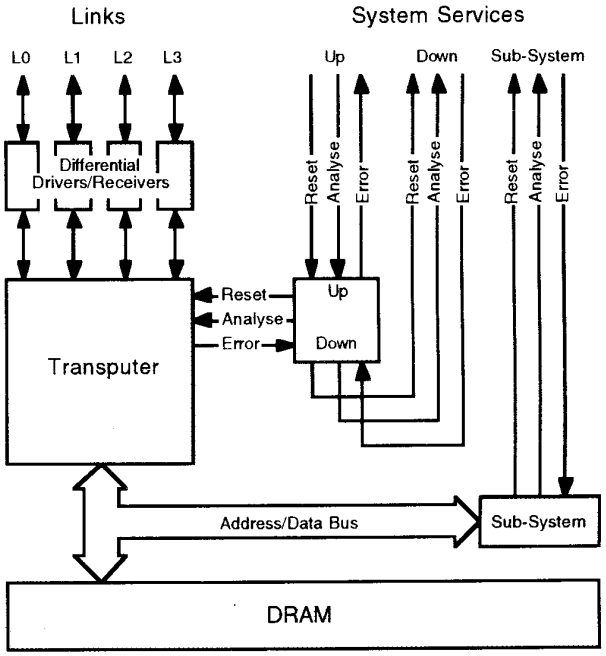
PART Number	Transputer Model	Transputer Speed	Memory Speed
PART.1-4(T40020-256K0)	T400	20 MHz	0 wait state
PART.1-4(T42520-256K0)	T425	20 MHz	0 wait state
PART.1-4(T80520-256K0)	T805	20 MHz	0 wait state
PART.1-4(T42525-256K1)	T425	25 MHz	1 wait state
PART.1-4(T80525-256K1)	T805	25 MHz	1 wait state

All models are delivered with:

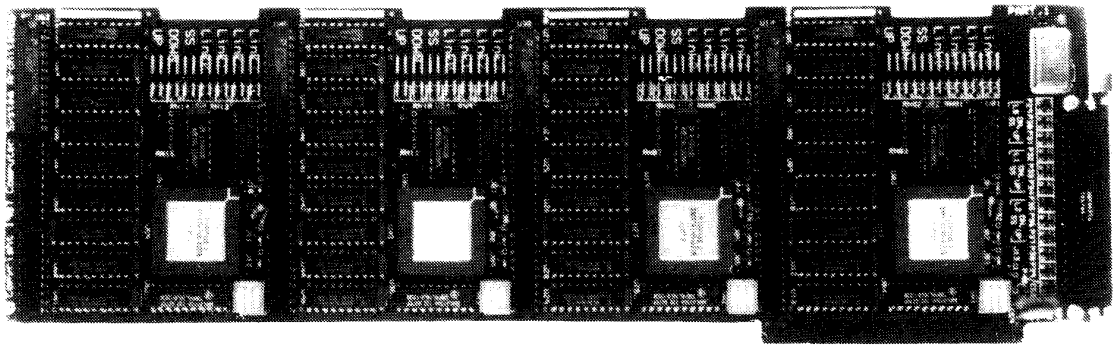
1. 14 PART.C1 Internal Signal Cables for link and system services interconnection within the same enclosure.
2. Diagnostics and sample programs on floppy disk.
3. Documentation package.

Power Requirements

2.5 A @ 5.0 V (typical)



One of the 4 Identical Processors



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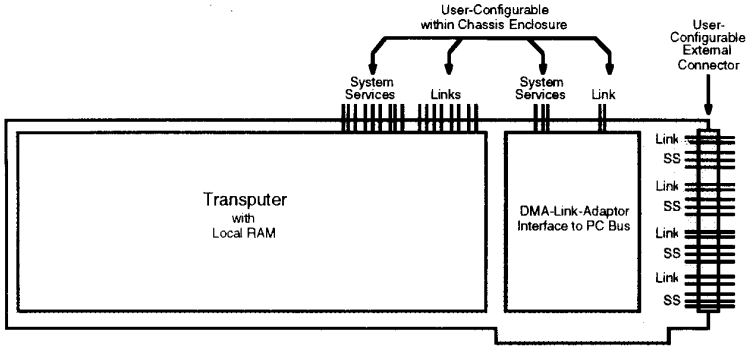
PART.5

with 4, 8, 16, or 32 MB of DRAM

Transputer Board with DMA-Link-Adaptor Interface to a PC-Bus



Description

CSA's PART.5 is a single processor computing module which can be plugged directly in, as a coprocessor, to an IBM PC, XT or AT bus. Compatible host processors include IBM PC's, APOLLO workstations having an AT bus and the Sun 386i.

The PART.5 circuitry consists of a 32-bit transputer with 4, 8, 16, or 32 MB of local DRAM with parity checking, and an 8-bit parallel DMA interface from a transputer link to the PC bus.

The PART.5 board is useful for transputer evaluation, parallel processing experimentation, and application program development and execution using compilers distributed by CSA, Inmos, Logical Systems, 3L and others.

All four bidirectional pairs of transputer links, plus the single pair from the link adaptor, are brought to connector pins on the upper edge of the circuit board to facilitate possible interconnection to other CSA transputer products within the same enclosure. In addition, a connector is provided on the rear edge of the board through which four links can be connected to CSA PARTS boards in other cabinets. All links are differentially driven, providing reliable communication over distances in excess of 40 feet.

The transputer event request and acknowledge (or pending) signals are also differentially buffered and also brought to connectors along the upper edge of the board.

Finally, system services signals (reset, analyze, and error) for both the link adaptor and the transputer are available along the upper edge of the board along with the links. There are also four sets of system services pins provided on the external connector. All system services signals are thus user-configurable, making it possible for the host workstation (via the link adaptor), or the transputer, to act as a master; or for the transputer to become a daisy-chained slave in an arbitrarily large and diverse network of processors.

Features

- Inmos 32-bit transputer
  - Accomodates the T400, T425, or floating point T805
  - Accomodates 20, 25, or 30 MHz transputers
- 4, 8, 16, or 32 MegaBytes of DRAM with parity checking
- 8-bit parallel interface to PC bus
  - Programmed I/O or DMA
  - PC interrupt capability
  - Data transfer at greater than 200 KBytes/sec
- 5 bidirectional serial links
  - 4 links from the transputer; 1 from the link adaptor
  - 100% user configurable
  - Speed selectable to 20 Mbits/sec
  - Differentially buffered for greater reliability
- Programmable system services (reset, analyze, error)
  - Host can act as master to local or other processors
  - Transputer can act as master to other processors
- Plugs into a CSA chassis, or optionally into an IBM PC bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Compatible with Transputer Education Kit boards
- Compatible with Inmos evaluation boards

Options

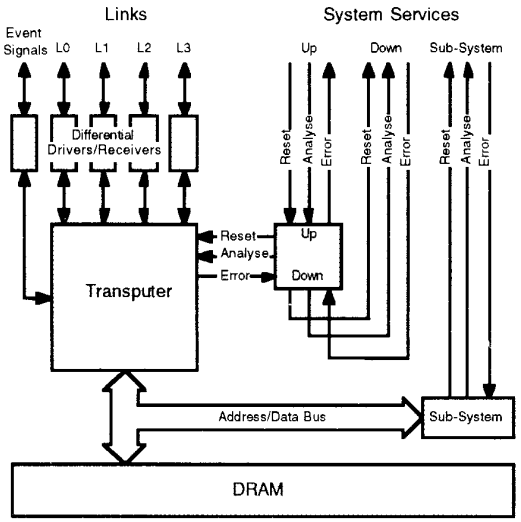
PART Number	Processor Model	Processor Speed	Memory Size	Memory Speed
PART.5-T40020-4M0	T400	20 MHz	4 MB	0 wait state
PART.5-T42520-4M0	T425	20 MHz	4 MB	0 wait state
PART.5-T80520-4M0	T805	20 MHz	4 MB	0 wait state
PART.5-T42525-4M0	T425	25 MHz	4 MB	1 wait state
PART.5-T80525-4M0	T805	25 MHz	4 MB	1 wait state
PART.5-T80530-4M1	T805	30 MHz	4 MB	2 wait state
PART.5-T40020-8M0	T400	20 MHz	8 MB	0 wait state
PART.5-T42520-8M0	T425	20 MHz	8 MB	0 wait state
PART.5-T80520-8M0	T805	20 MHz	8 MB	0 wait state
PART.5-T42525-8M0	T425	25 MHz	8 MB	1 wait state
PART.5-T80525-8M0	T805	25 MHz	8 MB	1 wait state
PART.5-T80530-8M1	T805	30 MHz	8 MB	2 wait state
PART.5-T40020-16M0	T400	20 MHz	16 MB	0 wait state
PART.5-T42520-16M0	T425	20 MHz	16 MB	0 wait state
PART.5-T80520-16M0	T805	20 MHz	16 MB	0 wait state
PART.5-T42525-32M0	T425	25 MHz	32 MB	1 wait state
PART.5-T80525-32M0	T805	25 MHz	32 MB	1 wait state

All models are delivered with:

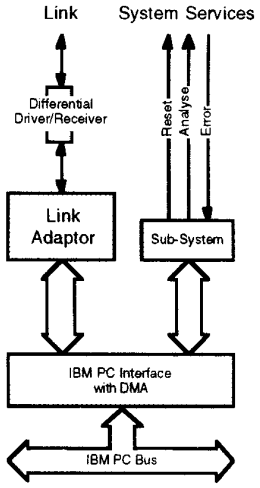
1. 6 PART.C1 Internal Signal Cables for link and system services interconnection within the same enclosure.
2. Diagnostics and sample programs on floppy disks.
3. Documentation package.

Power Requirements

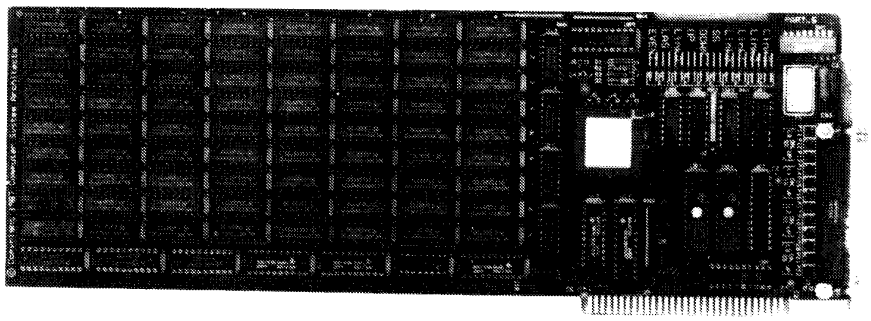
2.5 A @ 5.0 V (typical for PART.5 with 4 MB of DRAM)
2.8 A @ 5.0 V (typical for PART.5 with 8 MB of DRAM)
3.1 A @ 5.0 V (typical for PART.5 with 16 MB of DRAM)
3.5 A @ 5.0 V (typical for PART.5 with 32 MB of DRAM)



Processor Block Diagram



Link Adaptor Block Diagram



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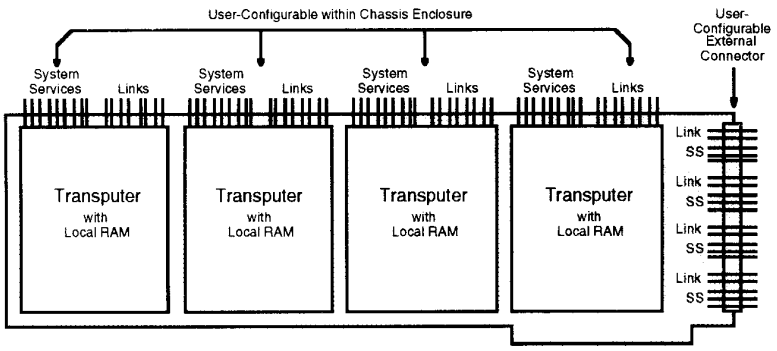
PART.6

1, 2, or 4 MB of DRAM per processor

Multi-Transputer Board
(with 1, 2, 3, or 4 processors)



Features

- 1, 2, 3 or 4 Inmos 32-bit transputers
  - Accomodates the T400, T425 or floating point T805
  - Accomodates 20, 25, or 30 MHz transputers
- 1, 2 or 4 MegaBytes of DRAM per transputer
- 16 bidirectional serial links
  - 4 links from each transputer
  - 100% user configurable
  - Speed selectable to 20 Mbits/sec
  - Differentially buffered for greater reliability
- Plugs into a CSA chassis, or optionally into an IBM PC bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Compatible with Transputer Education Kit boards
- Compatible with Inmos evaluation boards

Description

CSA's PART.6 is a multiprocessor computing module consisting of one, two, three or four 32-bit transputers, each with from 1, 2 or 4 MegaBytes of local DRAM.

All four links of each of the four transputers are brought to connector pins on the upper edge of the circuit board, allowing easy interconnection between processors on the same board or on other boards within the same enclosure. In addition, a connector is provided on the rear edge of the board through which up to four links can be connected to boards within other enclosures or cabinets.

All CSA links are differentially driven, guarantying reliable interconnection of devices over distances of 40 feet or more. Furthermore, CSA link signals are electrically terminated so that they can also be directly connected to raw TTL drivers and receivers as implemented on Inmos and several other manufacturers' boards.

In addition to functioning as a transputer with local RAM, each of the four processor nodes is capable of providing system services (i.e. of generating reset and analyze and of sensing error) via memory-mapped I/O circuitry. Thus any node can act as master to other nodes to which it might be interconnected.

System services signals for each of the four transputers are available along the upper edge of the board along with the links. There are also four sets of user-configurable system services pins provided on the external connector. Thus each of the transputers can be configured to act as a master or as a daisy-chined slave within an arbitrarily large network of processors.

PART.6 boards can be plugged into spare IBM PC card slots (they are not logically interfaced to the PC) or into an external desk-top or rack-mounted enclosure (see the PART.E4, PART.E6, or PART.E20). A logical interface to a host processor can be made via link interconnection through a CSA DMA-Link-Adaptor circuit as provided on various CSA PARTS boards (e.g. the PART.0, PART.4, PART.5, PART.8 or TEK.1).

The transputers on the PART.6 boards are configured to boot from link, and will accept code as generated by Inmos and most other vendor program development systems.

Options

PART Number	Transputer Model	Transputer Speed	Memory MB	Memory Speed
PART.6-4(T40020-1M0)	T400	20 MHz	4	0 wait state
PART.6-4(T42520-1M0)	T425	20 MHz	4	0 wait state
PART.6-4(T80520-1M0)	T805	20 MHz	4	0 wait state
PART.6-4(T42525-1M0)	T425	25 MHz	4	0 wait state
PART.6-4(T80525-1M0)	T805	25 MHz	4	0 wait state
PART.6-4(T80530-1M1)	T805	30 MHz	4	1 wait state
PART.6-4(T40020-2M0)	T400	20 MHz	8	0 wait state
PART.6-4(T42520-2M0)	T425	20 MHz	8	0 wait state
PART.6-4(T80520-2M0)	T805	20 MHz	8	0 wait state
PART.6-4(T42525-2M0)	T425	25 MHz	8	0 wait state
PART.6-4(T80525-2M0)	T805	25 MHz	8	0 wait state
PART.6-4(T80530-2M1)	T805	30 MHz	8	1 wait state
PART.6-4(T40020-4M0)	T400	20 MHz	16	0 wait state
PART.6-4(T42520-4M0)	T425	20 MHz	16	0 wait state
PART.6-4(T80520-4M0)	T805	20 MHz	16	0 wait state
PART.6-4(T42525-4M0)	T425	25 MHz	16	0 wait state
PART.6-4(T80525-4M0)	T805	25 MHz	16	0 wait state
PART.6-4(T80530-4M1)	T805	30 MHz	16	1 wait state

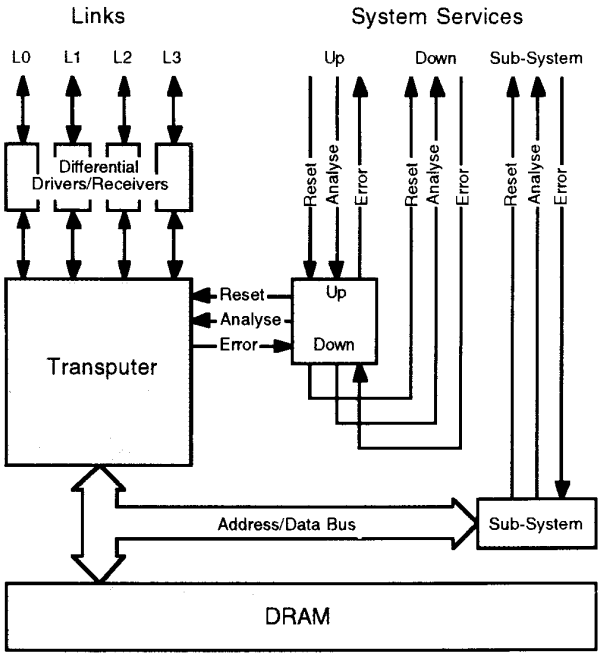
If ordering a partially populated board replace the numeral 4 (located to the right of the first dash in the part number) with a 1, 2 or 3, depending on the number of processors desired. For example, if ordering a half-populated board (only two processors) the part number might be PART.6-2(T80520-1M0).

All models are delivered with:

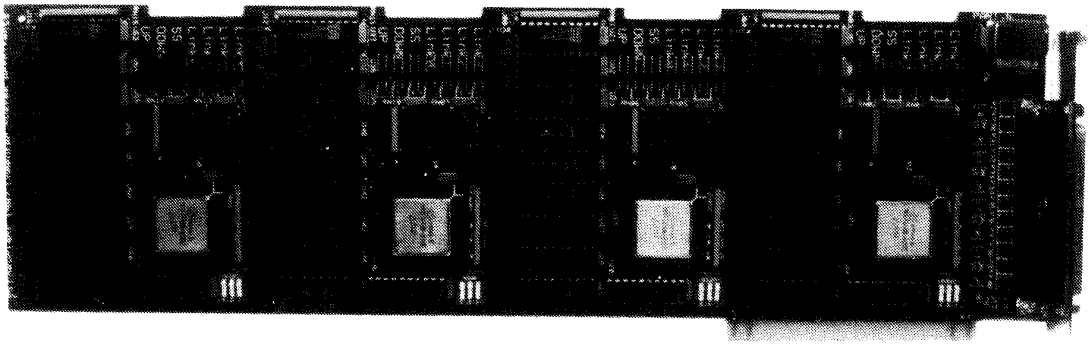
1. 14 PART.C1 Internal Signal Cables for link and system services interconnection within the same enclosure.
2. Diagnostics and sample programs on floppy disk.
3. Documentation package.

Power Requirements

3.0 A @ 5.0 V (typical for PART.6 with 4 MB DRAM)
4.0 A @ 5.0 V (typical for PART.6 with 8 MB DRAM)
4.0 A @ 5.0 V (typical for PART.6 with 16 MB DRAM)



One of the 4 Identical Processors



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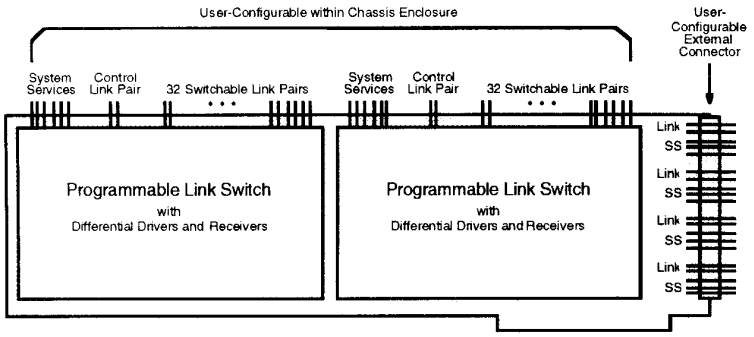
PART.7-1
single link switch

PART.7-2
dual link switches

Programmable Link Switch Board



Features

- User-configurable transputer link switch circuits
  - Incorporates the Inmos IMS C004 link switch
  - One switch on the PART.7-1 (half populated board)
  - Two identical switches on the PART.7-2
- 32 bidirectional links per switch
  - 32 links in; 32 links out
  - Any link pair can be connected to any other link pair
  - Up to 16 simultaneously active paths are possible
- Programmable control
  - Separate configuration control link
  - Simple configuration command format
- High speed
  - 10 or 20 Mbits/sec selectable data rate
  - Only 1.75 bit-time average through-switch latency
- High reliability
  - Differential drivers and receivers on all links
  - Cascadable with no loss of signal integrity
- Transparent to source and destination processors
  - No effect on data rate between transputers
  - No effect on hardware acknowledge
- Plugs into a CSA chassis, or optionally into an IBM PC bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Compatible with Inmos evaluation boards

Description

Functionally, the CSA PART.7-1 is just an Inmos IMS C004 programmable link switch chip mounted on an etched circuit board, and the PART.7-2 is just a pair of the same. The logical description of these circuits is exactly as presented in the Inmos data sheet for the C004. There are, however, two features which CSA has implemented which add significant value beyond simply placing the C004 pin-grid-array packages onto a circuit board: 1) differential drivers and receivers on every link pair, and 2) a highly reliable, user-configurable, physical interconnection mechanism (i.e. well-engineered connectors and cables).

Differential drivers and receivers assure reliable data transmission over distances in excess of 40 feet. Without such transmission line circuitry, (i.e. if link signals were wired directly to the transputer chip) data transmission could not be guaranteed reliable over distances beyond 20 to 30 inches. Even if buffered by conventional TTL drivers, data transfer between independently powered chassis, separated by only a foot or two, would be error prone. CSA's link driver and receiver circuitry has been designed so that, with special cabling, Inmos and other vendor transputer products can be directly interconnected with CSA products. However, improvements in reliability would, in this case, only occur between CSA devices.

All 32 bidirectional link pairs on each switch are brought up to miniature connectors along the top edge of the PART.7 circuit board, making it possible for the user to interconnect individual links stemming from any other CSA board within the same enclosure. Furthermore, a user-configurable external connector is provided along the rear edge of the board through which four links along with system services signals can be passed. This provides the possibility for interconnection to other cabinets via shielded, twisted-pair cabling.

In addition to connectors for the 32 links-to-be-switched (for each switch circuit), an up/down pair of system services connectors and a configuration control link connector are provided. The system services connectors (reset, analyze, and error) provide for a programmable switch reset and a means for transputer reset, analyze and error signals to be daisy-chained along to other boards. The configuration control link connector provides the mechanism by which the switch can be programmed or configured.

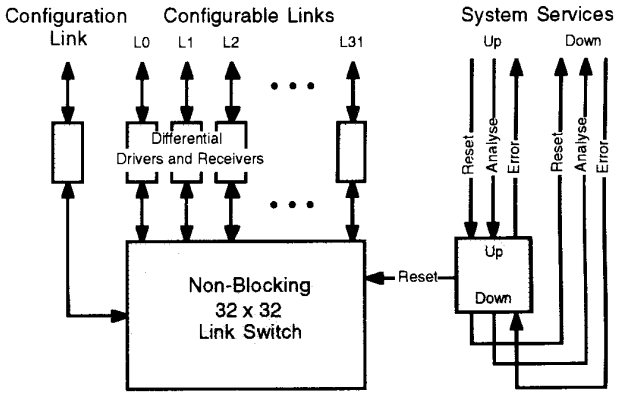
Switch configuration or reconfiguration occurs by way of simple command messages passed over the configuration control link. Command messages are not only simple, but short. A typical message might consist of a series of 3-byte link interconnection commands terminated by a 1-byte invoke command. Traffic in progress at the time of reconfiguration is unaffected by command messages pertaining to other link interconnections within the switch. However, should a reconfiguration command message specify disruption of a message in progress, both source and destination processes may lock up and require reinitialization.

Power Requirements

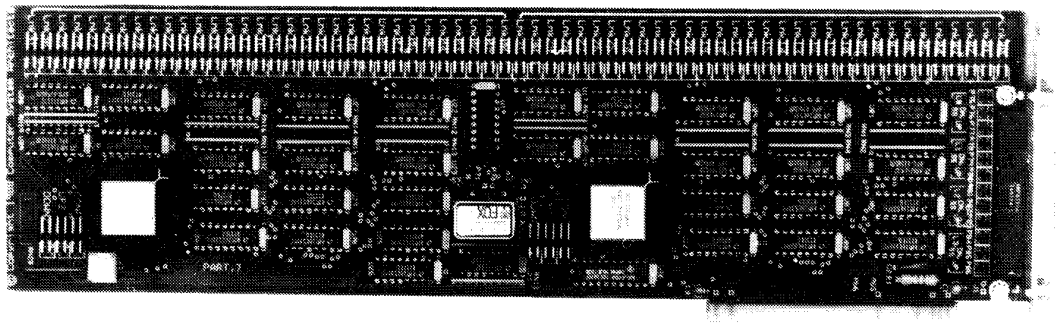
PART.7-1: 1.5 A @ 5.0 V (typical)
PART.7-2: 3.0 A @ 5.0 V (typical)

The CSA PART.7 is delivered with:

1. PART.C1 Internal Signal Cables (17 for the PART.7-1 and 34 for the PART.7-2) for link and system services interconnection within the same enclosure.
2. Diagnostics, subroutines, utilities, and sample programs on floppy disk.
3. Complete documentation package.



Programmable Link Switch Block Diagram



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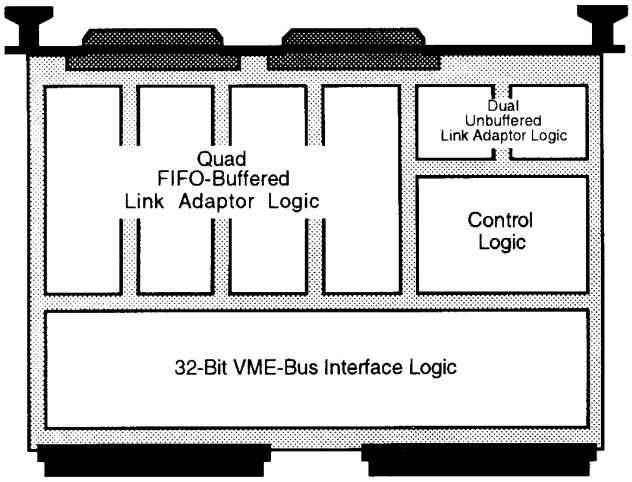
PART.8

Six Port
VME-bus to Link Adaptor Interface



Features

- 6 bidirectional transputer links
  - Four with FIFO buffers, two direct
  - Differential drivers/receivers for greater reliability
  - 10 or 20 megabits/sec transfer rate, selectable
  - Up to 1 megabyte/sec per link, unidirectional
  - Up to 2 megabytes/sec per link, bidirectional
  - Up to 10 megabytes/sec total for the interface
- 6 sets of programmable system services signals
  - Transputer reset and analyze outputs
  - Transputer error inputs
- 32-bit parallel interface to the VME-bus
  - Accomodates 8, 16, or 32 bit accesses
  - Accomodates block-transfer and DMA
  - Provides maskable interrupts to the VME host
  - 12 data ports (one in and one out for each link)
  - 6 control ports for transputer system services
  - Up to 20 megabytes/sec to/from FIFO buffers
- Plugs into standard 32-bit VME-bus (6U)
  - Compatible with Motorola, Apollo, and other
  - Compatible with SUN (6U to 9U adaptor available)
- Link and system services compatible with all other CSA PARTS products
- Link and system services compatible with Inmos Products (using optional adaptor cables)

Description

CSA's PART.8 is a parallel-to-serial/serial-to-parallel hex transputer link interface circuit on a standard VME-bus card. It is compatible with Motorola VME products, APOLLO workstations having a VME-bus, SUN-3 and SUN-4 workstations.

The PART.8 can be configured for either 16-bit or 32-bit data word lengths, and then accomodates either byte or full-word transfers. Addresses can be 16, 24 or 32 bits.

The circuitry functions as six pairs of independent ports; each pair consisting of one port going in each direction. Each port pair appears externally as a bidirectional transputer link with accompanying system services (transputer reset, analyze, and error). To the host processor, each port pair appears as two separate VME devices; one incoming and one outgoing.

Four of the six port pairs incorporate FIFO buffers which serve as speed matchers. The host processor can load (or empty) a FIFO via its VME interface at a much higher rate than can an external device operating over one of the transputer links -- by a factor of about 20 to 1. However, the host processor can access only one such device at a time. The transputer links, on the other hand, can all four be actively transferring data, each in both directions, simultaneously. The overall speed mismatch might, in some situations, be as close as about 2 to 1 (happily, in favor of the host processor). Thus, as the four transputer links simultaneously trickle data into and out of the FIFO's, the host processor can cycle around from FIFO to FIFO, loading or unloading entire blocks of data at a time.

For these four port pairs, the VME host can optionally use single word (or byte) programmed I/O transfers, block moves, or DMA control. The PART.8 provides a number of maskable interrupts which can notify the host on various conditions such as FIFO full, not full, half full, not empty or empty.

The two remaining port pairs are not equipped with FIFO buffers. The VME-bus sees them as byte-wide-only devices which are thus much slower than the aforementioned ports.

All six of the transputer links, each paired with a set of transputer system services signals, are combined within two 37-pin submini-D connectors along the front edge of the circuit board. These signals are also optionally available on the A and C pins of the VME P2 connector within the host chassis. Communication can thus occur between the VME host and a network of transputers (or other similarly interfaced hosts) located within an external chassis or within the host chassis itself. The provision of transputer system services signals makes it possible for the VME host to not only share data with one or more transputers, but to also act as a master to an arbitrarily large network of these processing nodes.

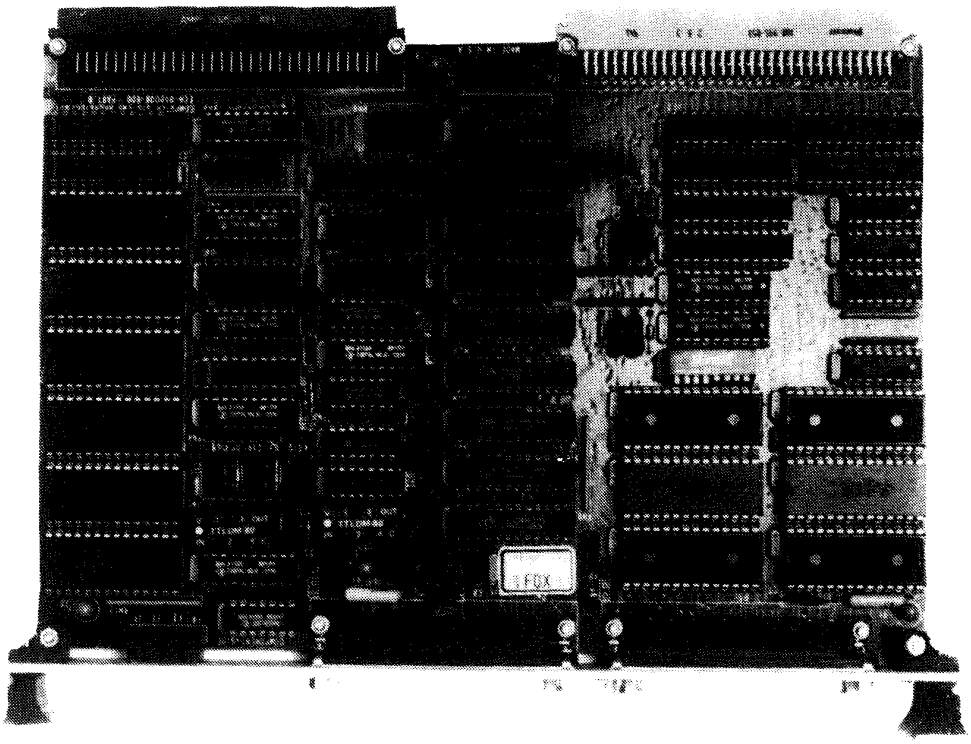
All six transputer links are differentially driven and received, providing guaranteed reliable transmission of data over distances in excess of 40 feet. The CSA PART.8 link circuitry is electrically terminated so that, with the use of optionally provided cables, it can be directly interconnected to other vendor's products.

The CSA PART.8 is delivered with:

1. Installation and theory of operation manual.
2. Floppy disk or tape cartridge containing diagnostics and sample programs. (Please specify type of host and preferred medium when ordering.)

Power Requirements

2 A @ 5.0 V (typical)



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PART.12-1
Single SCSI Controller

PART.12-2
Dual SCSI Controllers

Dual SCSI Controllers (with T222 Transputers)

Features

- One or two SCSI-bus controllers, each comprised of:
  - 20 MHz IMS T222 16-bit transputer
    - 4K bytes of 50 nsec on-chip SRAM
    - 4 differentially buffered, bidirectional serial links
  - 64K bytes of 2-processor-cycle off-chip SRAM
  - 5th bidirectional serial link (via programmed I/O)
  - High-speed SCSI-bus circuitry
    - Up to 5 megabytes/sec transfer rate to/from SCSI
    - Operates as Initiator for up to 7 target SCSI devices
    - Operate as SCSI target for host interconnection
    - Standard 50-pin internal SCSI connector
    - Mac-style 25-pin external SCSI connector
- User-programmable processor
  - The user can provide custom code for the T222, sourced in Occam2, Modula-2 or LS C: rev 89.1
  - Disk utilities provided include diagnostics, formatting, debugging and data recovery routines
  - Library processes include low-level access routines
  - Sockets are provided for optional EPROM
- Compatible with most SCSI peripherals.
- Compatible with host processors having SCSI interfaces, such as the Apple Macintosh.
- Plugs into a CSA chassis, or into an IBM PC or compatible, an APOLLO with a AT slots, or SUN 386i
- Compatible with all CSA PARTS boards (and other vendor products using optionally provided cables)

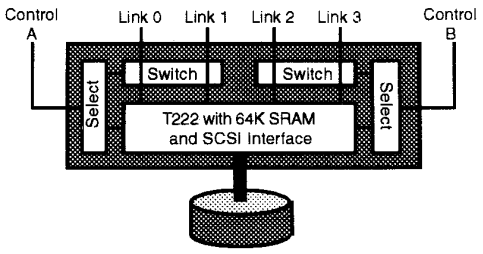
Description

CSA's PART.12 provides high-speed access to secondary store for the transputer user, or access to a transputer array from a SCSI host. Use of the SCSI standard makes available a wide selection of device types, capacities, and performance, ranging from small Winchester disks and backup tapes to the new WORM and CD ROM drives.

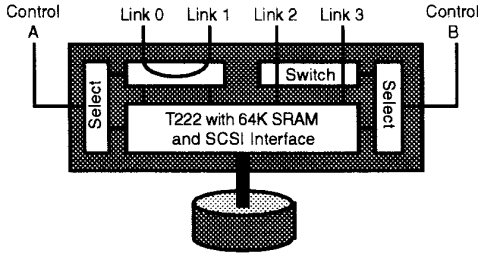
Using a T222 transputer with 64K bytes of SRAM and a FIFO-buffered interface to an SCSI-bus interface controller chip, the PART.12 provides: a) up to 5 megabytes of throughput to/from attached SCSI devices or host, b) high-speed execution of user application code, and c) five transputer serial links (four from the T222 plus a memory-mapped spare) by which the device can be externally accessed.

The data rate achievable over a transputer link closely matches the throughput of high performance storage devices. With five links there is more than adequate bandwidth to facilitate routing of data to appropriate destinations within a transputer network.

All 5 transputer links are equipped with differential drivers and receivers and brought to connector pins along the top edge of the circuit board, allowing easy interconnection with other processors within the same chassis. A unique feature of the PART.12 is the provision of a pair of 2-position link switches. When in the default "transparent" mode (see the following diagram) externally connected links go straight through the switch to the T222. (The spare



link is not involved here.) When either side of the switch is thrown (e.g. the A side, as depicted below), one pair of the



externally connected links logically bypasses the PART.12 circuit. In this way the PART.12 can be placed in-between two normally adjacent nodes, being switched-in only when one or the other of the two requires access to the disk.

The two switches, A and B, are independent of each other, and the PART.12 can be configured such that their control comes either directly from the two externally sourced control signals, Control-A and Control-B, or from the on-board T222 (possibly upon sensing the assertion of Control-A or Control-B). These externally sourced control signals could most likely be derived from the generally unused "subsystem" signals of any other CSA device, such as the PART.5 or PART.6.

Besides having the ability to communicate externally over the four transputer links (plus the spare link), the PART.12 is equipped with several sets of transputer system services signals (reset, analyze and error). There are the standard "up" and "down" sets as well as two "subsystem" sets. Of course "up" and "down" facilitate the daisy-chaining of system services signals from one device in a network to the next, while "subsystems" are under programmed control of the local T222. In fact Control-A and Control-B in the figures above are actually one and the same with these two sets of "subsystem" signals. All system services signals are brought to connector pins along the top edge of the circuit board, as has been stated as being the case for the serial links.

As for the SCSI-bus itself, two connectors are provided; a standard 50-pin connector for mounting of a SCSI device on the board itself (or elsewhere within the chassis), and on the rear I/O bracket, a 25-pin Macintosh-style connector for possible connection to one or more external-to-the-chassis SCSI units or a SCSI host.

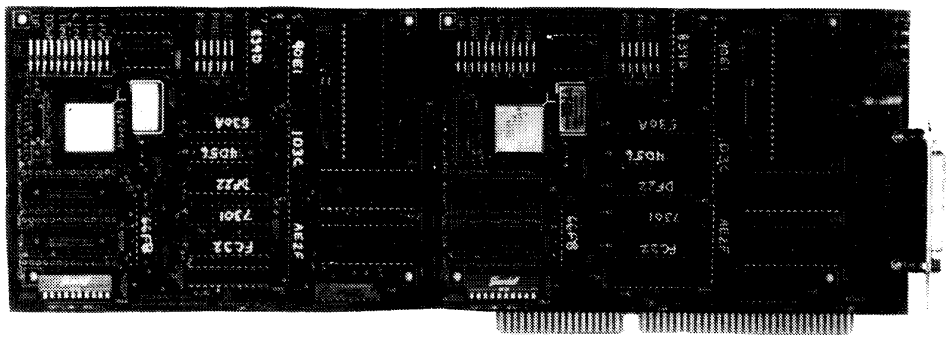
The PART.12 is optionally delivered with one or two on-board 100 or 200 megabyte Winchester disk drives. The board, with or without the on-board drive(s), fits in a standard CSA chassis, but is also compatible with the IBM PC/AT bus (using it only as a source of power and for mechanical support).

All models are delivered with:

1. 6 PART.C1 Internal Signal Cables for link and system services interconnection within the same enclosure.
2. Diagnostics, utilities, library routines, and sample programs on floppy disk.
3. Documentation package.

Power Requirements

PART.12-1 (Single Unit): 2.5 A @ +5.0 VDC (typical)
PART.12-2 (Dual Unit): 5.0 A @ +5.0 VDC (typical)



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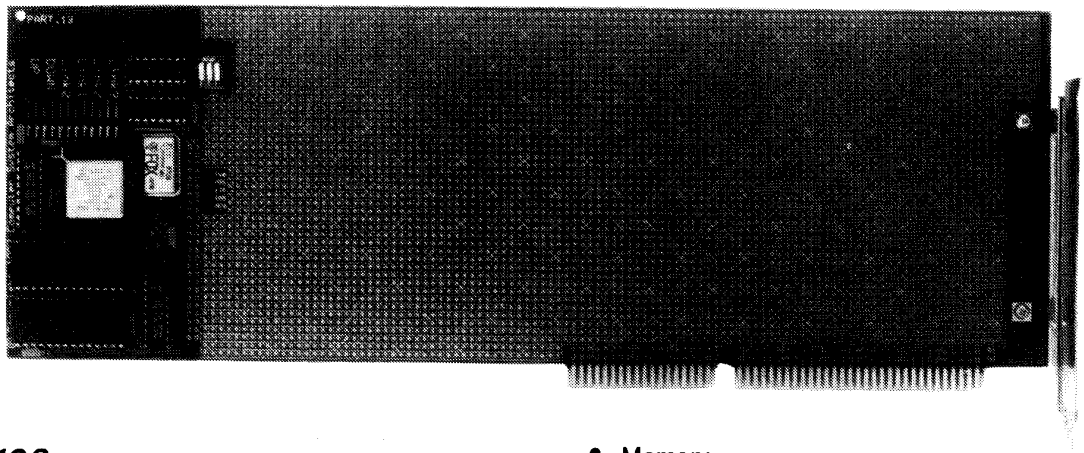
PART.13
for the PC/AT Bus

Prototyping Board with T222 Transputer



Features

- Inmos 16-Bit transputer (IMS T222-20)
  - High performance
    - 10 MIPS processor
    - Hardware support for multiple processes
    - Hardware scheduler with 2 priority levels
    - Sub-microsecond context switch
    - Sub-microsecond procedure calls
  - 4 high-speed, bidirectional serial links
    - 5, 10, or 20 megabits/second (selectable)
    - Links compatible with 32-bit transputer links
    - Up to 8.2 megabytes/sec total link data rate
    - Asynchronous (no common clock required)
    - Byte-level hardware handshaking
    - Program continues during DMA link transfers
  - Real-time and data acquisition capabilities
    - External event interrupt with acknowledge
    - Submicrosecond typical interrupt latency
    - 2 priority levels
    - Internal timers (resolution to 1 microsecond)
    - Optional memory wait states can be generated
  - 4K bytes of 50 Nanosecond on-chip SRAM
  - External memory interface
    - 16-bit with non-multiplexed address and data
    - 8 or 6 bit data accesses (selectable on the fly)
    - Up to 20 megabytes/sec memory bandwidth
  - Bootstraps from link or user-programmed PROM
  - Support for run-time error analysis
  - Single 5 VDC power supply required
- Memory
  - 64K bytes of off-chip SRAM provided
    - 2 processor cycle access (minimum possible)
    - 56K bytes accessible (as shipped)
  - Sockets provided for up to 32K bytes of PROM
    - 24K bytes accessible using jumpers
- CSA transputer link enhancements
  - Differential transmitters/receivers on all 4 links
    - Reliable within or between chassis
  - Miniature link cabling mechanism for flexible interconnection within the same chassis
- System services signals (reset, analyze, and error)
  - Programmable from upstream processor
  - Daisy-chainable to downstream processor(s)
  - Miniature cabling mechanism as with links
- Interface to user's prototype circuits
  - 2 memory-mapped-I/O address spaces reserved
    - 4K bytes for zero wait-state accesses
    - 4K bytes for one-or-more wait-state accesses
  - Connection points for 45 transputer signals
    - 16 address lines
    - 16 data I/O lines
    - 8 lines for memory-mapped-I/O control signals
    - 2 lines for interrupt request and acknowledge
    - 1 line to specify bootstrap source (link or ROM)
    - 1 transputer error line
    - 1 processor clock output (20 MHz)

- Prototyping area
  - More than 40 square inches: Holes on 0.1" grid
    4394 plated-through holes
    Accepts wire-wrap sockets
    Accepts BICC-Vero Speedwire terminals
    Accepts Robinson Nugent Quick/Connect sockets
  - 4-layer board
    Internal power and ground planes
    External power and ground grids
    138 vias to power plane, evenly distributed
    135 vias to ground plane, evenly distributed
    Less than 0.4" from any pin to power or ground
  - Connector to PC/AT-bus
    B1 and B31 are tied to ground
    B3 and B29 are tied to VCC
    Other bus pins are brought to vias; uncommitted
  - Provision for connector on rear edge of board
- Plugs into a CSA chassis, or optionally into an IBM PC-bus, an APOLLO AT slot, or a Sun 386i
- Compatible with all other CSA PARTS boards
- Programmable in Occam2, Modula-2, C, or Assembler

Description

CSA's PART.13 prototyping board consists of an Inmos IMS T222 16-bit transputer node placed at one end of a high-quality, well-designed prototyping board. Besides the fact that it possesses all the standard transputer features, the T222 is ideal in that it has separate address and data buses, is capable of accessing external RAM (or memory-mapped-I/O prototype circuitry) with a 100 nsec cycle time, and can directly accommodate either 8 or 16-bit memory, or memory-mapped-I/O data.

The device is configured at the factory with 64K bytes of SRAM (56K addressable), and 8K bytes of memory-mapped-I/O prototype address space (4K for zero wait-state accesses and 4K for one-or-more wait-state accesses. A number of jumper blocks have been provided so that the user can easily change configurations. Furthermore, several convenient cut-and-Jumper points have been provided, should some less likely configuration be desired. Finally, every signal trace has been routed along one of the exterior board layers, making it possible to change the circuit in the most unexpected manner. This board was made for the engineer/designer who desires the ultimate in convenience and flexibility.

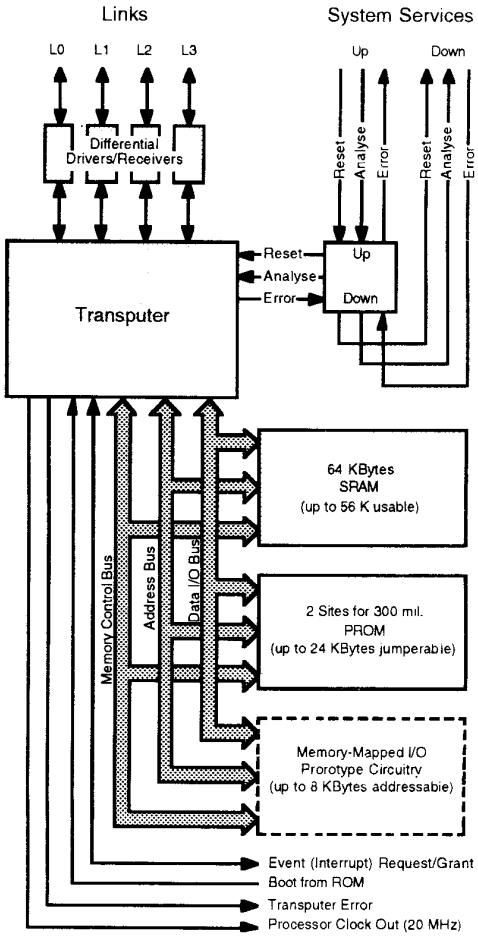
The PART.13 is exceptionally well suited to high-performance data acquisition applications.

The PART.13 is delivered with:

1. 3 PART.C1 Internal Signal Cables for link and system services interconnection within the chassis.
2. Diagnostics and sample programs on floppy disk.
3. Documentation package including schematics.

Power Requirements

0.6 A @ 5.0 V (typical without user prototype circuitry)



Prototyping Board Block Diagram

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